Datasheet | Rev. 1.8 | 2011

MEM2G04D2DABG 512Mx4 (64M x 4 x 8 Banks)
MEM2G08D2DABG 256Mx8 (32M x 8 x 8 Banks)
MEM2G16D2DABG 128Mx16 (16M x 16 x 8 Banks)

2Gbit Double-Data-Rate-Two SDRAM DDR2 SDRAM
RoHS Compliant Products

Revision History

Version: Rev. 1.8, FEB 2011

Typing errors corrected in Ball Descriptions/Assignment

Version: Rev. 1.7, DEC 2010

Revision 1.7: 1066 MHz speed-grade added

Version: Rev. 1.6, NOV 2010

Minimum value for t_{RFC} corrected to 195ns

Version: Rev. 1.5, NOV 2010

Industrial temperature (-40 to +95°C) option added

Version: Rev. 1.4, OCT 2010

Content-index added

Version: Rev. 1.3, OCT 2010

Changed T_{OPER} to T_{CASE} in Table 19. Fixed some typing errors.

Version: Rev. 1.2, SEP 2010

Fixed some minor non-technical errors

Version: Rev. 1.1, SEP 2010

Removed DDR2-667 CL5 and DDR2-800 CL6 ordering codes as these speed/latency requirements are all covered by the DDR2-800 CL5 type

Previous Version: Rev. 1.0, SEP 2010

Initialized version

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1 | Overview

This chapter gives an overview of the 2Gbit Double-Data-Rate-Two SDRAM product family and describes its main characteristics.

1.1 Features

- 1.8 V ± 0.1 V Power Supply
- 1.8 V ± 0.1 V (SSTL_18) compatible I/O
- DRAM organizations with 4, 8, 16 data in/outputs
- Double Data Rate architecture:
- two data transfers per clock cycle
- eight internal banks for concurrent operation
- Programmable CAS Latency: 3, 4, 5, 6 and 7
- Programmable Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Bi-directional, differential data strobes (DQS and $\overline{\text{DQS}}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and $\overline{\text{DQS}}$ transitions with clock
- $\overline{\text{DQS}}$ can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto- precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Operating temperature range 0°C to 95°C. Industrial temperature devices (Ordering code ending with "I") allow an operating temperature range of -40°C to 95°C
- Average Refresh Period 7.8µs at T_{CASE} lower than 85°C. For T_{CASE} between 85°C and 95°C a Refresh Period of 3.9µs is required
- Programmable self-refresh rate via EMRS2 setting
- DCC enabling via EMRS2 setting
- Full and reduced Strength Data-Output Drivers
- 1KB page size for ×4 and x8, 2KB page size for x16
- Packages: TFBGA-60 (x4, x8), TFBGA-84 (x16)
- RoHS Compliant Products [1]
- All Speed grades faster than DDR2–400 comply with DDR2–400 timing specifications when run at a clock rate of 200 MHz.

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[1] RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit http://www.memphis.ag

Table 1 - Performance Table

					Unit	Note
Speed Code			-25	-18		
Max. Data Rate		DDR2	-800	-1066	MHz	
CAS-RCD-RP latencies			5-5-5	7-7-7	t_{CK}	
Max. Clock Frequency	CL3	f_{CK3}	200	200	MHz	
	CL4	f_{CK4}	266	266	MHz	
	CL5	f_{CK5}	400	400	MHz	
	CL6	f_{CK6}	400	400	MHz	
	CL7	f_{CK7}	400	533	MHz	
Min. RAS-CAS-Delay		t_{RCD}	12.5	12.5	ns	
Min. Row Precharge Time		t_{RP}	12.5	12.5	ns	
Min. Row Active Time		t_{RAS}	45	45	ns	
Min. Row Cycle Time		t_{RC}	57.5	57.5	ns	
Precharge-All (8 banks) command period		t_{PREA}	15	15	ns	[1] [2]

[1] This t_{PREA} value is the minimum value at which this chip will be functional.

[2] Precharge-All command for an 8 bank device will equal to t_{RP} + 1 × t_{CK} or t_{nRP} + 1 × nCK, depending on the speed bin, where t_{nRP} = RU{ t_{RP} / $t_{CK(avg)}$ } and t_{RP} is the value for a single bank precharge.

1.2 Description

The 2Gbit DDR2 DRAM is a high-speed Double-Data-Rate- Two CMOS Synchronous DRAM device containing 2,147,483,648 bits and internally configured as an octal bank DRAM.

The 2Gbit device is organized as 64 Mbit ×4 I/O ×8 banks or 32 Mbit ×8 I/O ×8 banks or 16 Mbit ×16 I/O ×8 banks chip. These synchronous devices achieve high speed transferrates starting at 400 Mb/sec/pin for general applications. See Table 1 for performance figures.

The device is designed to comply with all DDR2 DRAM key features:

1. Posted $\overline{CAS}$ with additive latency.
2. Write latency = read latency - 1.
3. Normal and weak strength data-output driver.
4. Off-Chip Driver (OCD) impedance adjustment.
5. On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS-$\overline{DQS}$ pair in a source synchronous fashion.

A 18 bit address bus for x4 and x8 organized component and a 17 bit address bus for ×16 component is used to convey row, column and bank address information in a $\overline{RAS}$- $\overline{CAS}$ multiplexing style.

The DDR2 device operates with a 1.8 V ± 0.1 V power supply. An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR2 SDRAM is available in TFBGA package

Table 2 - Ordering Information for RoHS Compliant Products

Product Part Number [1]	Org.	Max. Speed	CAS-RCD-RP Latencies [2] [3] [4]	Max. Clock (MHz)	Package	Note
Standard Temperature Range (0°C to 95°C)						
MEM2G04D2DABG-18	×4	DDR2-1066	7-7-7	533	TFBGA-60	5
MEM2G08D2DABG-18	×8	DDR2-1066	7-7-7	533	TFBGA-60	5
MEM2G16D2DABG-18	×16	DDR2-1066	7-7-7	533	TFBGA-84	5
MEM2G04D2DABG-25	×4	DDR2-800	5-5-5	400	TFBGA-60	5
MEM2G08D2DABG-25	×8	DDR2-800	5-5-5	400	TFBGA-60	5
MEM2G16D2DABG-25	×16	DDR2-800	5-5-5	400	TFBGA-84	5
Industrial Temperature Range (-40°C to 95°C)						
MEM2G04D2DABG-25I	×4	DDR2-800	5-5-5	400	TFBGA-60	5
MEM2G08D2DABG-25I	×8	DDR2-800	5-5-5	400	TFBGA-60	5
MEM2G16D2DABG-25I	×16	DDR2-800	5-5-5	400	TFBGA-84	5

[1] For detailed information regarding the part numbering of Memphis products, please contact Memphis for a separated "Part No. Decoder".
[2] CAS: Column Address Strobe
[3] RCD: Row Column Delay
[4] RP: Row Precharge
[5] RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit http://www.memphis.ag

1.3 Addressing

Table 3 - Addressing

Configuration	512 Mb x 4 [1]	256 Mb x8 [2]	128 Mb x16 [3]	Note
Bank Address	BA[2:0]	BA[2:0]	BA[2:0]	
Number of Banks	8	8	8	
Auto Precharge	A10 / AP	A10 / AP	A10 / AP	
Row Address	A[14:0]	A[14:0]	A[13:0]	
Column Address	A[9:0], A11	A[9:0]	A[9:0]	
Number of Column Address Bits	11	10	10	4
Number of I/Os	4	8	16	
Page Size [Bytes]	1024 (1 K)	1024 (1 K)	2048 (2 K)	5

Notes:

[1] Referred to as 'org'
[2] Referred to as 'org'
[3] Referred to as 'org'
[4] Referred to as 'colbits'
[5] PageSize = $2^{\text{colbits}} \times \text{org}/8$ [Bytes]

2 | Configuration

This chapter contains the chip configuration. (CK)\bar

2.1 Configuration for TFBGA-60

The chip configuration of a DDR2 SDRAM is listed by function in Table 3. The abbreviations used in the Ball# and Buffer Type column are explained in Table 4 and Table 5 respectively.

Table 4 - BALL DESCRIPTION FOR TFBGA-60

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals x4/×8 Organizations				
E8	CK	I	SSTL	Clock Signal CK, bCK
F8	$\overline{CK}$	I	SSTL	
F2	CKE	I	SSTL	Clock Enable
Control Signals x4/×8 Organizations				
F7	$\overline{RAS}$	I	SSTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
G7	$\overline{CAS}$	I	SSTL	
F3	$\overline{WE}$	I	SSTL	
G8	$\overline{CS}$	I	SSTL	Chip Select
Address Signals x4/×8 Organizations				
G2	BA0	I	SSTL	Bank Address Bus 2:0
G3	BA1	I	SSTL	
G1	BA2	I	SSTL	
H8	A0	I	SSTL	Address Signal 14:0, Address Signal 10/Auto Precharge
H3	A1	I	SSTL	
H7	A2	I	SSTL	
J2	A3	I	SSTL	
J8	A4	I	SSTL	
J3	A5	I	SSTL	
J7	A6	I	SSTL	
K2	A7	I	SSTL	
K8	A8	I	SSTL	
K3	A9	I	SSTL	
H2	A10	I	SSTL	
	AP	I	SSTL	
K7	A11	I	SSTL	
L2	A12	I	SSTL	
L8	A13	I	SSTL	
L3	A14	I	SSTL	

Ball#	Name	Ball Type	Buffer Type	Function
Data Signals x4/×8 Organizations				
C8	DQ0	I/O	SSTL	Data Signal 3:0
C2	DQ1	I/O	SSTL	
D7	DQ2	I/O	SSTL	
D3	DQ3	I/O	SSTL	
D1	DQ4	I/O	SSTL	Data Signal 7:4
D9	DQ5	I/O	SSTL	
B1	DQ6	I/O	SSTL	
B9	DQ7	I/O	SSTL	
Data Strobe x4/×8 Organizations				
B7	DQS	I/O	SSTL	Data Strobe
A8	$\overline{DQS}$	I/O	SSTL	
Data Strobe ×8 Organization				
B3	RDQS	O	SSTL	Read Data Strobe
A2	$\overline{RDQS}$	O	SSTL	
Data Mask x4/×8 Organizations				
B3	DM	I	SSTL	Data Mask
Power Supplies x4 Organization				
A9, C1, C3, C7, C9	V_{DDQ}	PWR	–	I/O Driver Power Supply
A1, E9, H9, L1	V_{DD}	PWR	–	Power Supply
A7, B2, B8, D2, D8	V_{SSQ}	PWR	–	I/O Driver Power Supply
A3, J1,K9,E3	V_{SS}	PWR	–	Power Supply
E2	V_{REF}	AI	–	I/O Reference Voltage
E1	V_{DDL}	PWR	–	Power Supply
E7	V_{SSDL}	PWR	–	Power Supply
Power Supplies ×8 Organization				
A9, C1, C3, C7, C9	V_{DDQ}	PWR	–	I/O Driver Power Supply
A1, E9, H9, L1	V_{DD}	PWR	–	Power Supply
A7, B2, B8, D2, D8	V_{SSQ}	PWR	–	I/O Driver Power Supply
A3, J1,E3, K9	V_{SS}	PWR	–	Power Supply
E2	V_{REF}	AI	–	I/O Reference Voltage
E1	V_{DDL}	PWR	–	Power Supply
E7	V_{SSDL}	PWR	–	Power Supply
Not Connected ×4 Organization				
A2, B1, B9, D1,D9, L7	NC	NC	–	Not Connected
Not Connected ×8 Organization				
L7	NC	NC	–	Not Connected
Other Balls x4/×8 Organizations				
F9	ODT	I	SSTL	On-Die Termination Control

Table 5 - Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 6 - Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR allows multiple devices to share as a wire-OR.

Figure 1 - Ball Assignment for ×8 Components, TFBGA-60 (top view)

1	2	3	4	5	6	7	8	9
V_{DD}	NU/$\overline{RDQS}$	V_{SS}		A		V_{SSQ}	$\overline{DQS}$	V_{DDQ}
DQ6	V_{SSQ}	DM/RDQS		B		DQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		C		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		D		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		E		V_{SSDL}	CK	V_{DD}
	CKE	$\overline{WE}$		F		$\overline{RAS}$	$\overline{CK}$	ODT
BA2	BA0	BA1		G		$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1		H		A2	A0	V_{DD}
V_{SS}	A3	A5		J		A6	A4	
	A7	A9		K		A11	A8	V_{SS}
V_{DD}	A12	A14		L		NC	A13	

Notes:

1. RDQS/$\overline{RDQS}$are enabled by EMRS(1) command.
2. If RDQS/$\overline{RDQS}$ is enabled, the DM function is disabled.
3. When enabled, RDQS & /$\overline{RDQS}$ are used as strobe signals during reads.
4. V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{SSDL} is connected to V_{SS} internally. V_{DD}, V_{DDQ} and V_{SSQ} are isolated on the device.

Figure 2 - Ball Assignment for ×4 Components, TFBGA-60 (top view)

1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	$\overline{DQS}$	V_{DDQ}
NC	V_{SSQ}	DM		B		DQS	V_{SSQ}	NC
V_{DDQ}	DQ1	V_{DDQ}		C		V_{DDQ}	DQ0	V_{DDQ}
NC	V_{SSQ}	DQ3		D		DQ2	V_{SSQ}	NC
V_{DDL}	V_{REF}	V_{SS}		E		V_{SSDL}	CK	V_{DD}
	CKE	$\overline{WE}$		F		$\overline{RAS}$	$\overline{CK}$	ODT
BA2	BA0	BA1		G		$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1		H		A2	A0	V_{DD}
V_{SS}	A3	A5		J		A6	A4	
	A7	A9		K		A11	A8	V_{SS}
V_{DD}	A12	A14		L		NC	A13	

Notes:

5. RDQS/$\overline{RDQS}$are enabled by EMRS(1) command.
6. If RDQS/$\overline{RDQS}$ is enabled, the DM function is disabled.
7. When enabled, RDQS & /$\overline{RDQS}$ are used as strobe signals during reads.
8. V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{SSDL} is connected to V_{SS} internally. V_{DD}, V_{DDQ} and V_{SSQ} are isolated on the device.

2.2 Configuration for TFBGA-84

The chip configuration of a DDR2 SDRAM is listed by function in Table 6. The abbreviations used in the Ball#/Buffer Type columns are explained in Table 7 and Table 8 respectively.

Table 7 - BALL DESCRIPTION FOR TFBGA-84

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals ×16 Organization				
J8	CK	I	SSTL	Clock Signal CK, CK
K8	$\overline{CK}$	I	SSTL	
K2	CKE	I	SSTL	Clock Enable
Control Signals ×16 Organization				
K7	$\overline{RAS}$	I	SSTL	Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)
L7	$\overline{CAS}$	I	SSTL	
K3	$\overline{WE}$	I	SSTL	
L8	$\overline{CS}$	I	SSTL	Chip Select
Address Signals ×16 Organization				
L2	BA0	I	SSTL	Bank Address Bus 2:0
L3	BA1	I	SSTL	
L1	BA2	I	SSTL	
M8	A0	I	SSTL	Address Signal 13:0, Address Signal 10/Auto Precharge
M3	A1	I	SSTL	
M7	A2	I	SSTL	
N2	A3	I	SSTL	
N8	A4	I	SSTL	
N3	A5	I	SSTL	
N7	A6	I	SSTL	
P2	A7	I	SSTL	
P8	A8	I	SSTL	
P3	A9	I	SSTL	
M2	A10	I	SSTL	
	AP	I	SSTL	
P7	A11	I	SSTL	
R2	A12	I	SSTL	
R8	A13	I	SSTL	

Ball#	Name	Ball Type	Buffer Type	Function
Data Signals ×16 Organization				
G8	DQ0	I/O	SSTL	Data Signal Lower Byte 7:0
G2	DQ1	I/O	SSTL	
H7	DQ2	I/O	SSTL	
H3	DQ3	I/O	SSTL	
H1	DQ4	I/O	SSTL	
H9	DQ5	I/O	SSTL	
F1	DQ6	I/O	SSTL	
F9	DQ7	I/O	SSTL	
C8	DQ8	I/O	SSTL	Data Signal Upper Byte 15:8
C2	DQ9	I/O	SSTL	
D7	DQ10	I/O	SSTL	
D3	DQ11	I/O	SSTL	
D1	DQ12	I/O	SSTL	
D9	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
B9	DQ15	I/O	SSTL	
Data Strobe ×16 Organization				
B7	UDQS	I/O	SSTL	Data Strobe Upper Byte
A8	$\overline{UDQS}$	I/O	SSTL	
F7	LDQS	I/O	SSTL	Data Strobe Lower Byte
E8	$\overline{LDQS}$	I/O	SSTL	
Data Mask ×16 Organization				
B3	UDM	I	SSTL	Data Mask Upper Byte
F3	LDM	I	SSTL	Data Mask Lower Byte
Power Supplies ×16 Organization				
J2	V_{REF}	AI	–	I/O Reference Voltage
A9, C1, C3, C7, C9, E9, G1, G3, G7, G9	V_{DDQ}	PWR	–	I/O Driver Power Supply
J1	V_{DDL}	PWR	–	Power Supply
A1, E1, J9, M9, R1	V_{DD}	PWR	–	Power Supply
A7, B2, B8, D2, D8, E7, F2, F8, H2, H8	V_{SSQ}	PWR	–	Power Supply
J7	V_{SSDL}	PWR	–	Power Supply
A3, E3, J3, N1, P9	V_{SS}	PWR	–	Power Supply
Not Connected ×16 Organization				
A2, E2, R3, R7	NC	NC	–	Not Connected
Other Balls ×16 Organization				
K9	ODT	I	SSTL	On-Die Termination Control

Table 8 - Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

Table 9 - Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

Figure 3 - Ball Assignment for x16 Components, TFBGA-84 (top view)

1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	$\overline{\text{UDQS}}$	V_{DDQ}
DQ14	V_{SSQ}	UDM		B		UDQS	V_{SSQ}	DQ15
V_{DDQ}	DQ9	V_{DDQ}		C		V_{DDQ}	DQ8	V_{DDQ}
DQ12	V_{SSQ}	DQ11		D		DQ10	V_{SSQ}	DQ13
V_{DD}	NC	V_{SS}		E		V_{SSQ}	$\overline{\text{LDQS}}$	V_{DDQ}
DQ6	V_{SSQ}	LDM		F		LDQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		G		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		H		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		J		VSSDL	CK	V_{DD}
	CKE	$\overline{\text{WE}}$		K		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
BA2	BA0	BA1		L		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1		M		A2	A0	V_{DD}
V_{SS}	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	V_{SS}
V_{DD}	A12	NC		R		NC	A13	

Notes:

1. UDQS/$\overline{\text{UDQS}}$ is data strobe for DQ[15:8], LDQS/$\overline{\text{LDQS}}$ is data strobe for DQ[7:0]
2. LDM is the data mask signal for DQ[7:0], UDM is the data mask signal for DQ[15:8]
3. V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{SSDL} is connected to V_{SS} internally. V_{DD}, V_{DDQ} and V_{SSQ} are isolated on the device.

3 | Functional Description

This chapter contains the functional description.

3.1 Mode Register Set (MRS)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM.

BA2	BA1	BA0	A14–	A13	A12	A11 A10 A9	A8	A7	A6 A5 A4	A3	A2 A1 A0
0	0	0	0	0	PD	WR	DLL	TM	CL	BT	BL
reg. addr					W	W	W	W	W	W	W

Table 10 - Mode Register Definition, $BA_{2:0} = 000_B$

Field	Bits	Type[1]	Description
BA2	17	reg. addr.	Bank Address 2 0B BA2 Bank Address
BA1	16		Bank Address 1 0B BA1 Bank Address
BA0	15		Bank Address 0 0B BA0 Bank Address
A14	14		Address Bus 0B A14 Address bit 14
A13	13		Address Bus 0B A13 Address bit 13
PD	12	w	Active Power-Down Mode Select 0B PD Fast exit 1B PD Slow exit
WR	[11:9]	w	Write Recovery[2] Note: All other bit combinations are illegal. 001B WR 2 010B WR 3 011B WR 4 100B WR 5 101B WR 6
DLL	8	w	DLL Reset 0B DLL No 1B DLL Yes
TM	7	w	Test Mode 0B TM Normal Mode 1B TM Vendor specific test mode
CL	[6:4]	w	CAS Latency Note: All other bit combinations are illegal. 011_B CL 3 100_B CL 4 101_B CL 5 110_B CL 6 111_B CL 7
BT	3	w	Burst Type 0_B BT Sequential 1_B BT Interleaved
BL	[2:0]	w	Burst Length Note: All other bit combinations are illegal. 010_B BL 4 011_B BL 8

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[1] w = write only register bits

[2] Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WR [cycles] ≥ t_{WR} (ns) / t_{CK} (ns). The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing. WR_{MIN} is determined by $t_{CK.MAX}$ and WR_{MAX} is determined by $t_{CK.MIN}$.

3.2 Extended Mode Register EMR(1)

The Extended Mode Register EMR(1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, OCD program, ODT, DQS and output buffers disable, RDQS and RDQS enable.

BA2	BA1	BA0	A14–A13	A12	A11	A10	A9 A8 A7	A6	A5 A4 A3	A2	A1	A0
0	0	1	0	Q off	RDQS	DQS	OCD Program	R_{tt}	AL	R_{tt}	DIC	DLL
	reg. addr				w	w	w	w	w	w	w	w

Table 11 - Extended Mode Register Definition, $BA_{2:0}$ = 001_B

Field	Bits	Type[1]	Description
BA2	17	reg. addr.	**Bank Address 2** 0_B **BA2** Bank Address
BA1	16		**Bank Address 1** 0_B **BA1** Bank Address
BA0	15		**Bank Address 0** 1_B **BA0** Bank Address
A14	14	w	**Address Bus** 0_B **A14** Address bit 14
A13	13	w	**Address Bus** 0_B **A13** Address bit 13
Qoff	12	w	**Output Disable** 0_B **QOff** Output buffers enabled 1_B **QOff** Output buffers disabled
RDQS	11	w	**Read Data Strobe Output (RDQS, RDQS)** 0_B **RDQS** Disable 1_B **RDQS** Enable
$\overline{DQS}$	10	w	**Complement Data Strobe (DQS Output)** 0_B $\overline{\mathbf{DQS}}$ Enable 1_B $\overline{\mathbf{DQS}}$ Disable
OCD Program	[9:7]	w	**Off-Chip Driver Calibration Program** 000_B **OCD** OCD calibration mode exit, maintain setting 001_B **OCD** Drive (1) 010_B **OCD** Drive (0) 100_B **OCD** Adjust mode 111_B **OCD** OCD calibration default
AL	[5:3]	w	Additive Latency Note: All other bit combinations are illegal. 000_B **AL** 0 001_B **AL** 1 010_B **AL** 2 011_B **AL** 3 100_B **AL** 4 101_B **AL** 5 110_B **AL** 6 111_B **Reserved**
R_{TT}	6,2	w	**Nominal Termination Resistance of ODT** Note: See Table 21 “ODT DC Electrical Characteristics” 00_B **RTT** ∞ (ODT disabled) 01_B **RTT** 75 Ohm 10_B **RTT** 150 Ohm 11_B **RTT** 50 Ohm
DIC	1	w	**Off-chip Driver Impedance Control** 0_B **DIC** Full (Driver Size = 100%) 1_B **DIC** Reduced
DLL	0	w	**DLL Enable** 0_B **DLL** Enable 1_B **DLL** Disable

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[1] w = write only register bits

3.3 Extended Mode Register EMR(2)

The Extended Mode Registers EMR(2) and EMR(3) are reserved for future use and must be programmed when setting the mode register during initialization.

BA2	BA1	BA0	A14-13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0						SRF	0			DCC	PASR		

Reg. addr

Table 12 - EMR(2) Programming Extended Mode Register Definition, BA $_{2:0}$=010$_B$

Field	Bits	Type[1]	Description
BA2	17	reg. addr.	**Bank Address** 0_B **BA2** Bank Address
BA	[16:15]		**Bank Address** 00_B **BA** MRS 01_B **BA** EMRS(1) 10_B **BA** EMRS(2) 11_B **BA** EMRS(3): Reserved
A	[14:8]	w	**Address Bus** 0000000_B **A** Address bits
SRF	7	w	**Address Bus, High Temperature Self Refresh Rate for T_{CASE} > 85°C** 0_B **A7** disable 1_B **A7** enable [2]
A	[6:4]	w	**Address Bus** 0000_B **A** Address bits
DCC	3	w	**Address Bus, Duty Cycle Correction (DCC)** 0_B **A3** DCC disabled 1_B **A3** DCC enabled
Partial Self Refresh for 8 banks [3]			

[1] w = write only

[2] When DRAM is operated at 85°C ≤ T_{CASE} ≤ 95°C the extended self-refresh rate must be enabled by setting bit A7 to 1 before the self-refresh mode can be entered.

[3] Not supported by this product

3.4 Extended Mode Register EMR(3)

The Extended Mode Register EMR(3) is reserved for future use and all bits except BA0 and BA1 must be programmed to 0 when setting the mode register during initialization.

BA2	BA1	BA0	A14-13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0													

Reg. addr

Table 13 - EMR(3) Programming Extended Mode Register Definition, BA $_{2:0}$=011$_B$

Field	Bits	Type [1]	Description
BA2	17	reg.addr	**Bank Address 2** 0_B **BA2** Bank Address
BA1	16		**Bank Address 1** 1_B **BA1** Bank Address
BA0	15		**Bank Address 0** 1_B **BA0** Bank Address
A	[14:0]	W	**Address Bus 14:0** 000000000000000_B**A[14:0]** Address bits

[1] w = write only

3.5 Burst Mode Operation

Table 14 - Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	× 0 0	0, 1, 2, 3	0, 1, 2, 3
	× 0 1	1, 2, 3, 0	1, 0, 3, 2
	×1 0	2, 3, 0, 1	2, 3, 0, 1
	×1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

4 | Truth Tables

The truth tables in this chapter summarize the commands and the signal coding to control a standard Double-Data-Rate-Two SDRAM.

Table 15 - Command Truth Table

Function	CKE		CS	RAS	CAS	WE	BA0 BA1 BA2	A[14:11]	A10	A[9:0]	Note [1] [2] [3]
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			4 5 6
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	4
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	4 7
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	4 7 8
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	4 5
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	4 5
Bank Activate	H	H	L	L	H	H	BA	Row Address			4 5
Write	H	H	L	H	L	L	BA	Column	L	Column	4 5 9
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	4 5 9
Read	H	H	L	H	L	H	BA	Column	L	Column	4 5 9
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	4 5 9
No Operation	H	X	L	H	H	H	X	X	X	X	4
Device Deselect	H	X	H	X	X	X	X	X	X	X	4
Power Down Entry	H	L	H	X	X	X	X	X	X	X	4 10
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	4 10
			L	H	H	H					

---

[1] The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.

[2] "X" means H or L (but a defined logic level).

[3] Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

[4] All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.

[5] Bank addresses BA[2:0] determine which bank is to be operated upon. For (E)MRS BA[2:0] selects an (Extended) Mode Register.

[6] All banks must be in a precharged idle state, CKE must be high at least for t_{XP} and all read/write bursts must be finished before the (Extended) Mode Register set Command is issued.

[7] V_{REF} must be maintained during Self Refresh operation.

[8] Self Refresh Exit is asynchronous.

[9] Burst reads or writes at BL = 4 cannot be terminated. See Chapter 3.5 for details.

[10] The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements

Table 16 - Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [1]	CKE		Command (N) [2] [3] RAS, CAS, WE, CS	Action (N) [2]	Note [4] [5]
	Previous Cycle [6] (N-1)	Current Cycle [6] (N)			
Power-Down	L	L	X	Maintain Power-Down	7 8 11
	L	H	DESELECT or NOP	Power-Down Exit	7 9 10 11
Self Refresh	L	L	X	Maintain Self Refresh	8 11 12
	L	H	DESELECT or NOP	Self Refresh Exit	9 11 12 13 14
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	7 9 10 11 15
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	9 10 11 15
	H	L	AUTOREFRESH	Self Refresh Entry	7 11 14 16
Any State other than listed above	H	H	Refer to the Command Truth Table		17

[1] Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.

[2] Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N).

[3] The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. .

[4] CKE must be maintained HIGH while the device is in OCD calibration mode.

[5] Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

[6] CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

[7] The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefore limited by the refresh requirements.

[8] “X” means “don’t care (including floating around V_{REF})” in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to 1 in EMRS(1)).

[9] All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

[10] Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.

[11] $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CK} + t_{IH}$.

[12] V_{REF} must be maintained during Self Refresh operation.

[13] On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.

[14] Valid commands for Self Refresh Exit are NOP and DESELCT only.

[15] Power-Down and Self Refresh cannot be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress.

[16] Self Refresh mode can only be entered from the All Banks Idle state.

[17] Must be a legal command as defined in the Command Truth Table.

Table 17 - Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1
Write Inhibit	H	X	

[1] Used to mask write data; provided coincident with the corresponding data

5 | Electrical Characteristics

This chapter describes the Electrical Characteristics.

5.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in Table 18 at any time.

Table 18 - Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-1.0	+2.3	V	1
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.5	+2.3	V	1 2
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	-0.5	+2.3	V	1 2
V_{IN} V_{OUT}	Voltage on any pin relative to V_{SS}	-0.5	+2.3	V	1
T_{STG}	Storage Temperature	-55	+100	°C	1 2

[1] When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

[2] Storage Temperature is the case surface temperature on the center/top side of the DRAM.

Attention:

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19 - DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
T_{CASE}	Operating Temperature for standard product	0	+95	°C	1 2 3 5 6 Standard
T_{CASE}	Operating Temperature for Industrial Temperature product	-40	+95	°C	1 2 4 5 6 Standard

[1] Operating Temperature is the case surface temperature on the center / top side of the DRAM.

[2] The operating temperature range are the temperatures where all DRAM specification will be supported.

[3] During operation, the DRAM case temperature must be maintained between 0 to 95°C under all other specification parameters.

[4] During operation, the DRAM case temperature must be maintained between -40 to 95°C under all other specification parameters.

[5] Above 85°C the Auto-Refresh command interval has to be reduced to tREFI= 3.9µs.

[6] When operating this product in the 85°C to 95°C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to 1. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%.

5.2 DC Characteristics

Table 20 - Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1
V_{DDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2 3
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	4

[1] V_{DDQ} tracks with V_{DD}, V_{DDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDL} tied together.

[2] The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about 0.5 × V_{DDQ} of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.

[3] Peak to peak ac noise on V_{REF} may not exceed ± 2% V_{REF} (dc)

[4] V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}

Table 21 - ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm	Rtt1(eff)	60	75	90	Ω	1
Termination resistor impedance value for EMRS(1)[A6,A2] = [1,0]; 150 Ohm	Rtt2(eff)	120	150	180	Ω	1
Termination resistor impedance value for EMRS(1)(A6,A2)=[1,1]; 50 Ohm	Rtt3(eff)	40	50	60	Ω	1 2
Deviation of V_M with respect to V_{DDQ} / 2	delta V_M	-6.00	–	+ 6.00	%	3

[1] Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IHac})$ and $I(V_{ILac})$ respectively Rtt(eff) = $(V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IHac}) - I(V_{ILac}))$.

[2] Mandatory for DDR2-800.

[3] Measurement Definition for V_M: Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: delta V_M = ((2 x VM / V_{DDQ}) –) 1 x 100%

Table 22 - Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current; any input 0 V < VIN < V_{DD}	–2	+2	µA	1
I_{OL}	Output Leakage Current; 0 V < VOUT < V_{DDQ}	–5	+5	µA	2

[1] All other pins not under test = 0 V

[2] DQ's, LDQS, $\overline{LDQS}$, UDQS, $\overline{UDQS}$, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$ are disabled and ODT is turned off

5.3 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) “Enable $\overline{\mathrm{DQS}}$” mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at VREF.

In differential mode, these timing relationships are measured relative to the cross point of $\overline{\mathrm{DQS}}$ and its complement, DQS. This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the $\overline{\mathrm{DQS}}$(and $\overline{\mathrm{RDQS}}$) signals are internally disabled and don’t care

Table 23 - DC & AC Logic Input Levels

Symbol	Parameter	DDR2 SDRAM-800		Units
		Min.	Max.	
$V_{IH(dc)}$	DC input logic HIGH	V_{REF} + 0.125	V_{DDQ} + 0.3	V
$V_{IL(dc)}$	DC input LOW	-0.3	V_{REF} – 0.125	V
$V_{IH(ac)}$	AC input logic HIGH	V_{REF} + 0.200	V_{DDQ} + V_{PEAK}	V
$V_{IL(ac)}$	AC input LOW	V_{SSQ} – V_{PEAK}	V_{REF} – 0.200	V

Table 24 - Single-ended AC Input Test Conditions

Symbol	Condition	Value	Unit	Notes
V_{REF}	Input reference voltage	0.5 × V_{DDQ}	V	1
$V_{SWING.MAX}$	Input signal maximum peak to peak swing	1.0	V	1
SLEW	Input signal minimum Slew Rate	1.0	V / ns	2 3

[1] Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.

[2] The input signal minimum Slew Rate is to be maintained over the range from $V_{IH(ac).MIN}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(ac).MAX}$ for falling edges as shown in Figure 4.

[3] AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions

Figure 4 - Single-ended AC Input Test Conditions Diagram

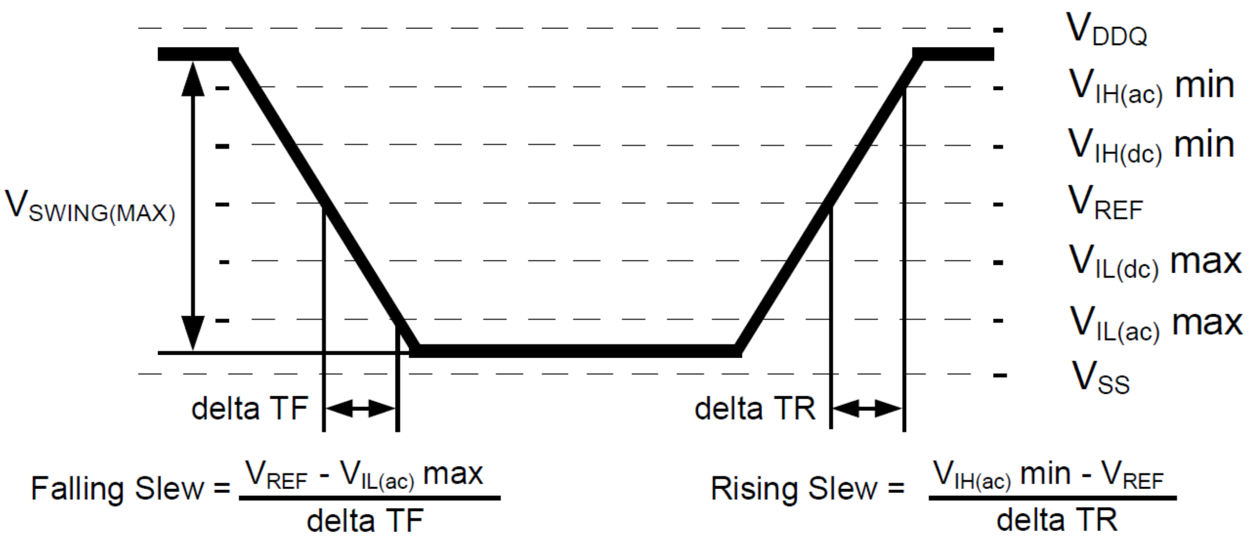


Table 25 - Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	Min.	Max.	Unit	Notes
$V_{IN(dc)}$	DC input signal voltage	-0.3	V_{DDQ} + 0.3	–	1
$V_{ID(dc)}$	DC differential input voltage	0.25	V_{DDQ} + 0.6	–	2
$V_{ID(ac)}$	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	3
$V_{IX(ac)}$	AC differential cross point input voltage	0.5 × V_{DDQ} – 0.175	0.5 × V_{DDQ} + 0.175	V	4
$V_{OX(ac)}$	AC differential cross point output voltage	0.5 × V_{DDQ} – 0.125	0.5 × V_{DDQ} + 0.125	V	5

[1] $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{CK}$, DQS, $\overline{DQS}$ etc.

[2] $V_{ID(dc)}$ specifies the input differential voltage V_{TR}– V_{CP} required for switching. The minimum value is equal to $V_{IH(dc)} - V_{IL(dc)}$.

[3] $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} - V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} - V_{IL(ac)}$.

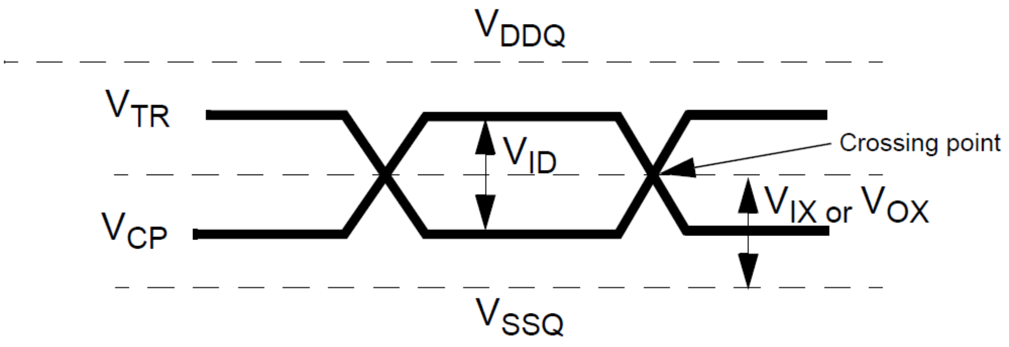
[4] The value of $V_{IX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ}. $V_{IX(ac)}$

[5] indicates the voltage at which differential input signals must cross.

[6] The value of $V_{OX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ}. $V_{OX(ac)}$

[7] indicates the voltage at which differential input signals must cross.

Figure 5 - Differential DC and AC Input and Output Logic Levels Diagram



5.4 Output Buffer Characteristics

This chapter describes the Output Buffer Characteristics.

Table 26 - SSTL_18 Output DC Current Drive

Symbol	Parameter	SSTL_18	Unit	Notes
I_{OH}	Output Minimum Source DC Current	–13.4	mA	[1] [2]
I_{OL}	Output Minimum Sink DC Current	13.4	mA	[2] [3]

[1] V_{DDQ} = 1.7 V; V_{OUT} = 1.42 V. (V_{OUT}-V_{DDQ}) / I_{OH} must be less than 21 Ω for values of V_{OUT} between V_{DDQ} and V_{DDQ} – 280 mV.

[2] The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in 1) and 3). They are used to test drive current capability to ensure $V_{IH.MIN}$. plus a noise margin and $V_{IL.MAX}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 Ohm load line to define a convenient current for measurement.

[3] V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT} / I_{OL} must be less than 21 Ohm for values of V_{OUT} between 0 V and 280 mV.

Table 27 - SSTL_18 Output AC Test Conditions

Symbol	Parameter	SSTL_18	Unit	Notes
V_{OH}	Minimum Required Output Pull-up	V_{TT} + 0.603	V	1
V_{OL}	Maximum Required Output Pull-down	V_{TT} – 0.603	V	1
V_{OTR}	Output Timing Measurement Reference Level	0.5 × V_{DDQ}	V	

[1] SSTL_18 test load for V_{OH} and V_{OL} is different from the referenced load . The SSTL_18 test load has a 20 Ohm series resistor additionally to the 25 Ohm termination resistor into V_{TT}. The SSTL_18 definition assumes that ± 335 mV must be developed across the effectively 25 Ohm termination resistor (13.4 mA × 25 Ohm = 335 mV). With an additional series resistor of 20 Ohm this translates into a minimum requirement of 603 mV swing relative to V_{TT}, at the output device (13.4 mA × 45 Ohm = 603 mV).

Table 28 - SSTL_18 Output AC Test Conditions

Symbol	Description	Min.	Nominal	Max.	Unit	Notes
–	Output Impedance				Ω	1 2
–	Pull-up / Pull down mismatch	0	–	4	Ω	1 2 3
–	Output Impedance step size for OCD calibration	0	–	1.5	Ω	4
S_{OUT}	Output Slew Rate	1.5	–	5.0	V / ns	1 5 6 7

[1] V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V

[2] Impedance measurement condition for output source dc current: V_{DDQ} = 1.7 V, V_{OUT} = 1420 mV; $(V_{OUT}–V_{DDQ}) / I_{OH}$ must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and V_{DDQ} – 280 mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 1.7 V; V_{OUT} = –280 mV; V_{OUT} / I_{OL} must be less than 23.4 Ohms for values of V_{OUT} between 0 V and 280 mV.

[3] Mismatch is absolute value between pull-up and pull-down, both measured at same temperature and voltage.

[4] This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is 18 ± 0.75 Ohms under nominal conditions.

[5] The absolute value of the Slew Rate as measured from DC to DC is equal to or greater than the Slew Rate as measured from AC to AC. This is verified by design and characterization but not subject to production test.

[6] Timing skew due to DRAM output Slew Rate mis-match between DQS/$\overline{DQS}$ and associated DQ's is included in t_{DQSQ} and t_{QHS} specification.

[7] DRAM output Slew Rate specification applies to 800 MT/s speed bins.

5.5 Input / Output Capacitance

This chapter contains the Input / Output Capacitance.

Table 29 - Input / Output Capacitance

Symbol	Parameter	DDR2-800		Unit
		Min.	Max.	
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	–	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	1.75	pF
CDI	Input capacitance delta, all other input- only pins	–	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$	–	0.5	pF

5.6 Overshoot and Undershoot Specification

This chapter contains Overshoot and Undershoot Specification.

Table 30 - AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2-800	Unit
Maximum peak amplitude allowed for overshoot area	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	V
Maximum overshoot area above V_{DD}	0.66	V-ns
Maximum undershoot area below V_{SS}	0.66	V-ns

Figure 6 - AC Overshoot / Undershoot Diagram for Address and Control Pins

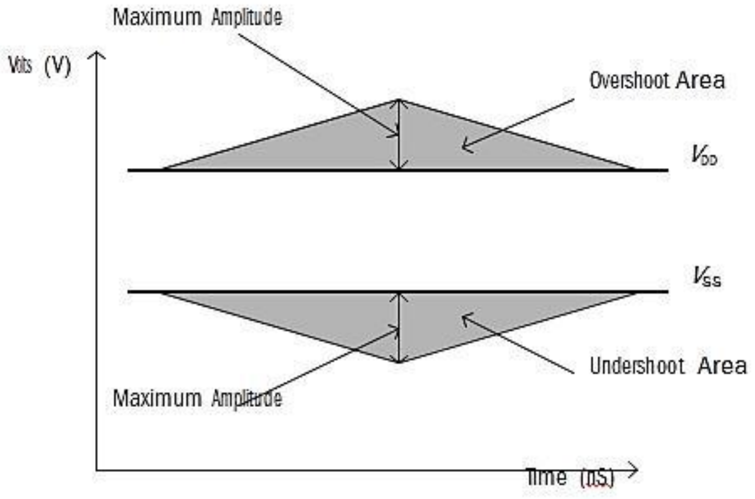
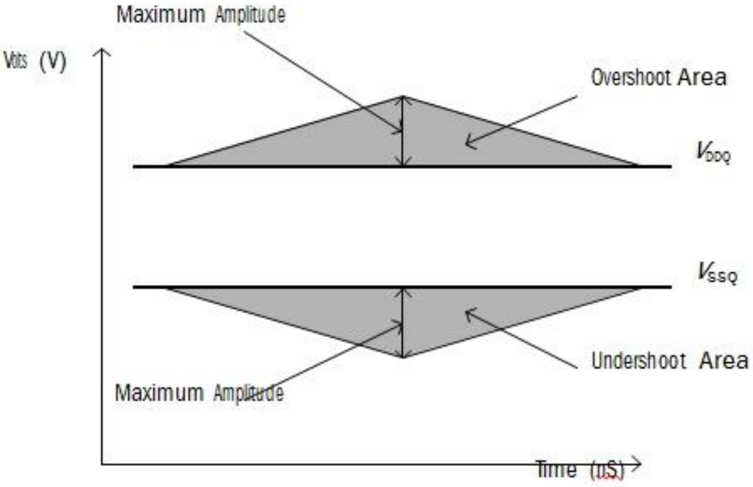


Table 31 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins

Parameter	DDR2-800	Unit
Maximum peak amplitude allowed for overshoot area	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	V
Maximum overshoot area above V_{DD}	0.23	V-ns
Maximum undershoot area below V_{SS}	0.23	V-ns

Figure 7 - AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Pins



6 | Currents Measurement Conditions

This chapter describes the Current Measurement, Specifications and Conditions

Table 32 - AC Overshoot / I_{DD} Measurement Conditions

Parameter	Symbol	Note
Operating Current - One bank Active - Precharge $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Data bus inputs are switching.	I_{DD0}	1 2 3 4 5 6
Operating Current - One bank Active - Read - Precharge I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$, AL = 0, CL = CL(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Data bus inputs are switching.	I_{DD1}	1 2 3 4 5 6
Precharge Power-Down Current All banks idle; CKE is LOW; $t_{CK} = t_{CK(IDD)}$;Other control and address inputs are stable; Data bus inputs are floating.	I_{DD2P}	1 2 3 4 5 6
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are switching, Data bus inputs are switching.	I_{DD2N}	1 2 3 4 5 6
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable, Data bus inputs are floating.	I_{DD2Q}	1 2 3 4 5 6
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, CKE is LOW; Other control and address inputs are stable; Data bus inputs are floating. MRS A12 bit is set to 0 (Fast Power-down Exit).	$I_{DD3P(0)}$	1 2 3 4 5 6
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, CKE is LOW; Other control and address inputs are stable, Data bus inputs are floating. MRS A12 bit is set to 1 (Slow Power-down Exit);	$I_{DD3P(1)}$	1 2 3 4 5 6
Active Standby Current All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD3N}	1 2 3 4 5 6
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX.(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching; I_{OUT} = 0 mA.	I_{DD4R}	1 2 3 4 5 6
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD4W}	1 2 3 4 5 6
Burst Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{RFC} = t_{RFC(IDD)}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5B}	1 2 3 4 5 6
Distributed Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every t_{REFI} = 7.8μs interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5D}	1 2 3 4 5 6
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are floating, Data bus inputs are floating.	I_{DD6}	1 2 3 4 5 6
Operating Bank Interleave Read Current 1. All banks interleaving reads, I_{OUT} = 0 mA; BL = 4, CL = $CL_{(IDD)}$, AL = $t_{RCD(IDD)}$ -1 × $t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RRD} = t_{RRD(IDD)}$; tFAW = tFAW(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address bus inputs are stable during deselects; Data bus is switching. 2. Timing pattern: see Detailed I_{DD7} timings shown below.	I_{DD7}	1 2 3 4 5 6

[1] V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V.

[2] I_{DD} specifications are tested after the device is properly initialized.

[3] I_{DD} parameter are specified with ODT disabled.

[4] Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.

[5] Definitions for I_{DD} , see Table 33.

[6] Timing parameter minimum and maximum values for I_{DD} current measurements are defined in Chapter 7.

Detailed I_{DD7}

The detailed timings are shown below for I_{DD7}. Changes will be required if timing parameter changes are made to the specification. Legend: A = Active; RA = Read with Auto precharge; D = Deselect.

I_{DD7} : Operating Current: All Bank Interleave Read operation

All banks are being interleaved at minimum $t_{RC.IDD}$ without violating $t_{RRD.IDD}$ and $t_{FAW.IDD}$ using a burst length of 4. Control and address bus inputs are STABLE during DESELECTs. IOUT = 0 mA.

Timing Patterns for devices with 1KB page size
DDR2-800: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D A4 RA4 D A5 RA5 D A6 RA6 D A7 RA7 D D D
Timing Patterns for devices with 2KB page size
DDR2-800: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D A4 RA4 D D A5 RA5 D D A6 RA6 D D A7 RA7 D D D D

Table 33 - Definition for I_{DD}

Parameter	Description
LOW	Defined as $V_{IN} \leq V_{IL.AC.MAX}$
HIGH	Defined as $V_{IN} \geq V_{IH.AC.MIN}$
STABLE	Defined as inputs are stable at a HIGH or LOW level
FLOATING	Defined as inputs are $V_{REF} = V_{DDQ} / 2$
SWITCHING	Defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or strobes

Table 34 - Preliminary[1] I_{DD} Specification

Symbol	DDR2 - 800	DDR2-1066	Unit	Note
	-25(I)	-18		
	Max.	Max.		
I_{DD0}	72	73	mA	x4/x8
I_{DD0}	83	85	mA	x16
I_{DD1}	80	82	mA	x4/x8
I_{DD1}	91	92	mA	x16
I_{DD2P}	12	12	mA	
I_{DD2N}	50	50	mA	
I_{DD2Q}	45	45	mA	
I_{DD3P_0} (fast)	16	16	mA	x4/x8
I_{DD3P_1} (slow)	16	16	mA	x4/x8
I_{DD3P_0} (fast)	16	16	mA	x16
I_{DD3P_1} (slow)	16	16	mA	x16
I_{DD3N}	55	55	mA	
I_{DD4R}	135	140	mA	x4/x8
I_{DD4R}	170	175	mA	x16
I_{DD4W}	120	125	mA	x4/x8
I_{DD4W}	150	155	mA	x16
I_{DD5B}	160	165	mA	
I_{DD5D}	16	16	mA	
I_{DD6}	12	12	mA	[1]
$I_{DD6\_hightemp}$	18	8	mA	[2]
I_{DD7}	200	210	mA	x4/x8
I_{DD7}	250	260	mA	x16

[1] Valid for 0°C ≤ T_{CASE} ≤ 95°C for the standard product and -40°C ≤ T_{CASE} ≤ 95°C for the industrial temperature product

[2] Above 85°C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9µs. When operating this product in the 85°C to 95°C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to 1. When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%, specified as $I_{DD6\_hightemp}$ here

7 | Timing Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

7.1 Speed Grade Definitions

Table 35 - Speed Grade Definition

Speed Grade			DDR2–800		DDR2-1066		Unit	Note
Speed Code			–25		-18			
CAS-RCD-RP latencies			5–5–5		7-7-7		t_{CK}	
Parameter		Symbol	Min.	Max.	Min.	Max.	–	
Clock Period	@ CL = 3	t_{CK}	5	8	5	8	ns	1 2 3 4
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1 2 3 4
	@ CL = 5	t_{CK}	2.5	8	2.5	8	ns	1 2 3 4
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1 2 3 4
	@ CL = 7	t_{CK}	1.875	8	2.5	8	Ns	1 2 3 4
Row Active Time		t_{RAS}	45	70k	45	70k	ns	1 2 3 4 5
Row Cycle Time		t_{RC}	57.5	–	57.5	—	ns	1 2 3 4
RAS-CAS-Delay		t_{RCD}	12.5	–	12.5	—	ns	1 2 3 4
Row Precharge Time		t_{RP}	12.5	–	12.5	—	ns	1 2 3 4

7.2 Component AC Timing Parameters

Table 36 - DRAM Component Timing Parameter by Speed Grade - DDR2–800 / DDR2-1066

Parameter	Symbol	DDR2-800		DDR2-1066		Unit	Note
		Min.	Max.	Min.	Max.		1 2 3 4 5 6 7
Row Active Time	t_{RAS}	45	70k	45	70k	ns	1 2 3 4 5
DQ output access time from CK / $\overline{CK}$	t_{AC}	-400	+400	–350	+350	ps	8
CAS to $\overline{CAS}$ command delay	t_{CCD}	2	–	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	0.48	0.52	$t_{CK.AVG}$	9 10
Average clock period	$t_{CK.AVG}$	2500	8000	1875	7500	ps	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	–	3	—	nCK	11
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	0.48	0.52	$t_{CK.AVG}$	9 10
Auto Precharge write recovery + Precharge time	t_{DAL}	WR + t_{nRP}	–	WR + t_{nRP}	—	nCK	12 13
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK.AVG} + t_{IH}$	--	$t_{IS} + t_{CK.AVG} + t_{IH}$	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	125	--	75	—	ps	14 18 19
DQ and DM input pulse width for each input	t_{DIPW}	0.35	–	0.35	—	$t_{CK.AVG}$	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	-350	+350	–325	+325	ps	8
DQS input high pulse width	t_{DQSH}	0.35	–	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	–	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	–	200	—	175	ps	15
DQS latching rising transition to associated clock edges	t_{DQSS}	- 0.25	+ 0.25	– 0.25	+ 0.25	$t_{CK.AVG}$	16
DQ and DM input setup time	$t_{DS.BASE}$	50	--	0	—	ps	17 18 19
DQS falling edge hold time from CK	t_{DSH}	0.2	–	0.2	—	$t_{CK.AVG}$	16
DQS falling edge to CK setup time	t_{DSS}	0.2	–	0.2	—	$t_{CK.AVG}$	16
Four Activate Window for 1KB page size products	t_{FAW}	35	–	35	—	ns	34
Four Activate Window for 2KB page size products	t_{FAW}	45	–	45	—	ns	34
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	–	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	20
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	–	$t_{AC.MAX}$	—	$t_{AC.MAX}$	ps	8 21
Address and control input hold time	$t_{IH.BASE}$	250	–	200	—	ps	22 24
Control & address input pulse width for each input	t_{IPW}	0.6	–	0.6	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	175	–	125	—	ps	23 24
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	2 × $t_{AC.MIN}$	$t_{AC.MAX}$	ps	8 21
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	8 21
MRS command to ODT update delay	t_{MOD}	0	12	0	12	ns	34

Parameter	Symbol	DDR2-800		DDR2-1066		Unit	Note [1] [2] [3] [4] [5] [6] [7]
		Min.	Max.	Min.	Max.		
Mode register set command cycle time	t_{MRD}	2	–	2	—	nCK	
OCD drive mode output delay	t_{OIT}	0	12	0	12	ns	[34]
DQ/DQS output hold time from DQS	t_{QH}	t_{HP} - t_{QHS}	–	t_{HP} – t_{QHS}	—	ps	[25]
DQ hold skew factor	t_{QHS}	–	300	—	250	ps	[26]
Average periodic refresh Interval	t_{REFI}	–	7.8	—	7.8	µs	[27] [28]
		–	3.9	—	3.9	µs	[27] [29]
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	195	–	197.5	—	ns	[30]
Read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	$t_{CK.AVG}$	[31] [32]
Read postamble	t_{RPST}	0.4	0.6	0.4	0.6	$t_{CK.AVG}$	[31] [33]
Active to active command period for 1KB page size products	t_{RRD}	7.5	–	7.5	—	ns	[34]
Active to active command period for 2KB page size products	t_{RRD}	10	–	10	—	ns	[34]
Internal Read to Precharge command delay	t_{RTP}	7.5	–	7.5	—	ns	[34]
Write preamble	t_{WPRE}	0.35	–	0.35	—	$t_{CK.AVG}$	
Write postamble	t_{WPST}	0.4	0.6	0.4	0.6	$t_{CK.AVG}$	
Write recovery time	t_{WR}	15	–	15	—	ns	[34]
Internal write to read command delay	t_{WTR}	7.5	–	7.5	—	ns	[34] [35]
Exit active power down to read command	t_{XARD}	2	–	3	—	nCK	
Exit active power down to read command (slow exit, lower power)	t_{XARDS}	8 – AL	–	10 – AL	—	nCK	
Exit Precharge power-down to any command	t_{XP}	2	–	2	—	nCK	
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	–	t_{RFC} +10	—	ns	[34]
Exit self-refresh to read command	t_{XSRD}	200	–	200	—	nCK	
Write command to DQS associated clock edges	WL	RL – 1		RL – 1		nCK	

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[1] $V_{DDQ} = 1.8\ V \pm 0.1V$; $V_{DD} = 1.8\ V \pm 0.1\ V$.

[2] Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

[3] Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode.

[4] The CK / CK input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the cross point when in differential strobe mode.

[5] Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.

[6] The output timing reference voltage level is V_{TT}.

[7] New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2-800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG} + t_{ERR.2PER(Min)}$.

[8] When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual $t_{ERR(6-10per)}$ of the input clock. (output de-ratings are relative to the SDRAM input clock.)

[9] Input clock jitter spec parameter. These parameters and the ones in Chapter 7.3 are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2-800 only. The jitter specified is a random jitter meeting a Gaussian distribution.

[10] These parameters are specified per their average values, however it is understood that the relationship as defined in Chapter 7.3 between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations of Chapter 7.3).

[11] $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

[12] DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.

[13] $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.

[14] Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe cross point to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe cross point to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, $\overline{DQS}$ signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See Figure 8.

[15] t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.

[16] These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

[17] Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe cross point for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe cross point for a falling signal applied to the device under test. DQS, $\overline{DQS}$ signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See Figure 8.

[18] If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.

[19] These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal (L/U/R) DQS / $\overline{DQS}$) crossing.

[20] t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} =MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.

[21] t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .

[22] input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test.
See Figure 9.

[23] Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test.
See Figure 9.

[24] These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

[25] t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.}

[26] t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers.

[27] The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85°C and 95°C.

[28] $0°C \le T_{CASE} \le 85°C$.

[29] $85°C < T_{CASE} \le 95°C$.

[30] A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x t_{REFI}.

[31] t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). Figure 7 shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

[32] When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual $t_{JIT.PER}$ of the input clock. (output de-ratings are relative to the SDRAM input clock.)

[33] When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual $t_{JIT.DUTY}$ of the input clock. (output de-ratings are relative to the SDRAM input clock.)

[34] For these parameters, the DDR2 SDRAM device is characterized and verified to support t_{nPARAM} = RU{t_{PARAM} / $t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met.

[35] t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

Figure 8 - Method for Calculating Transitions and Endpoint

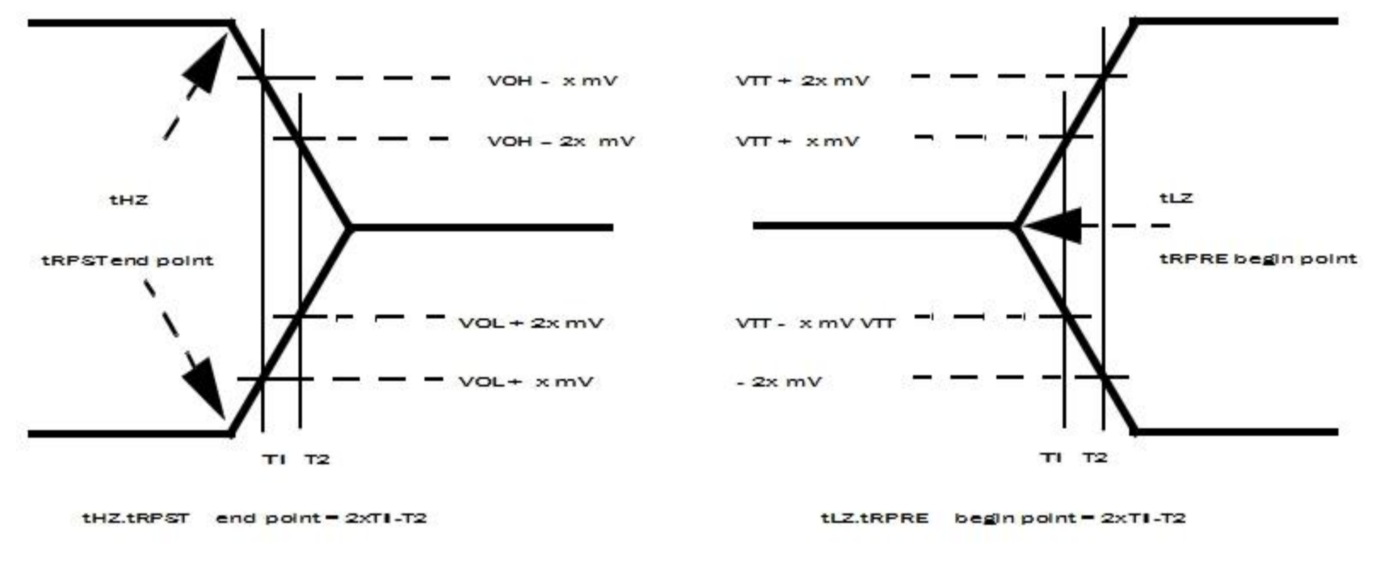


Figure 9 - Differential Input Waveform Timing - t_{DS} and t_{DH}

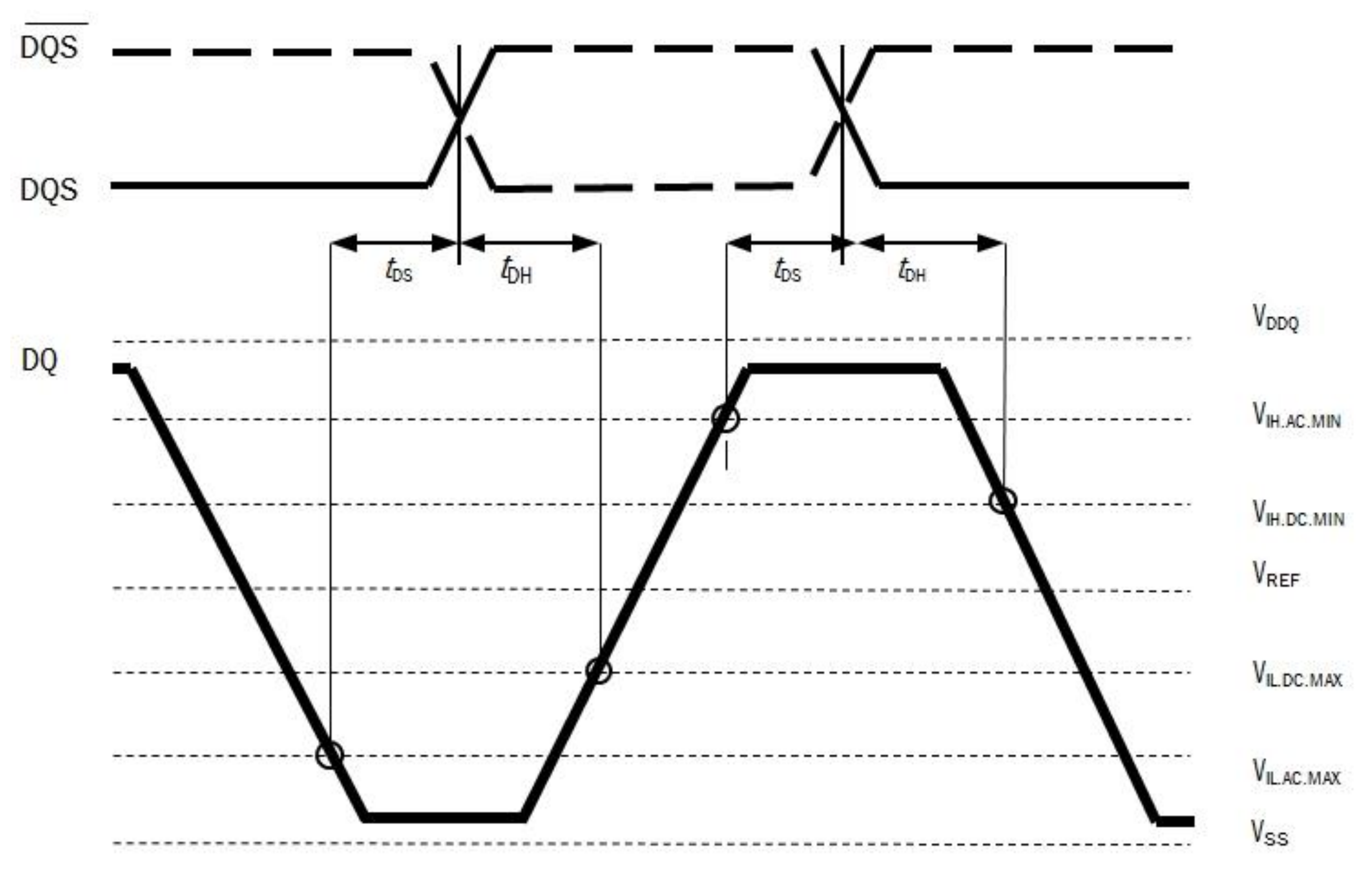
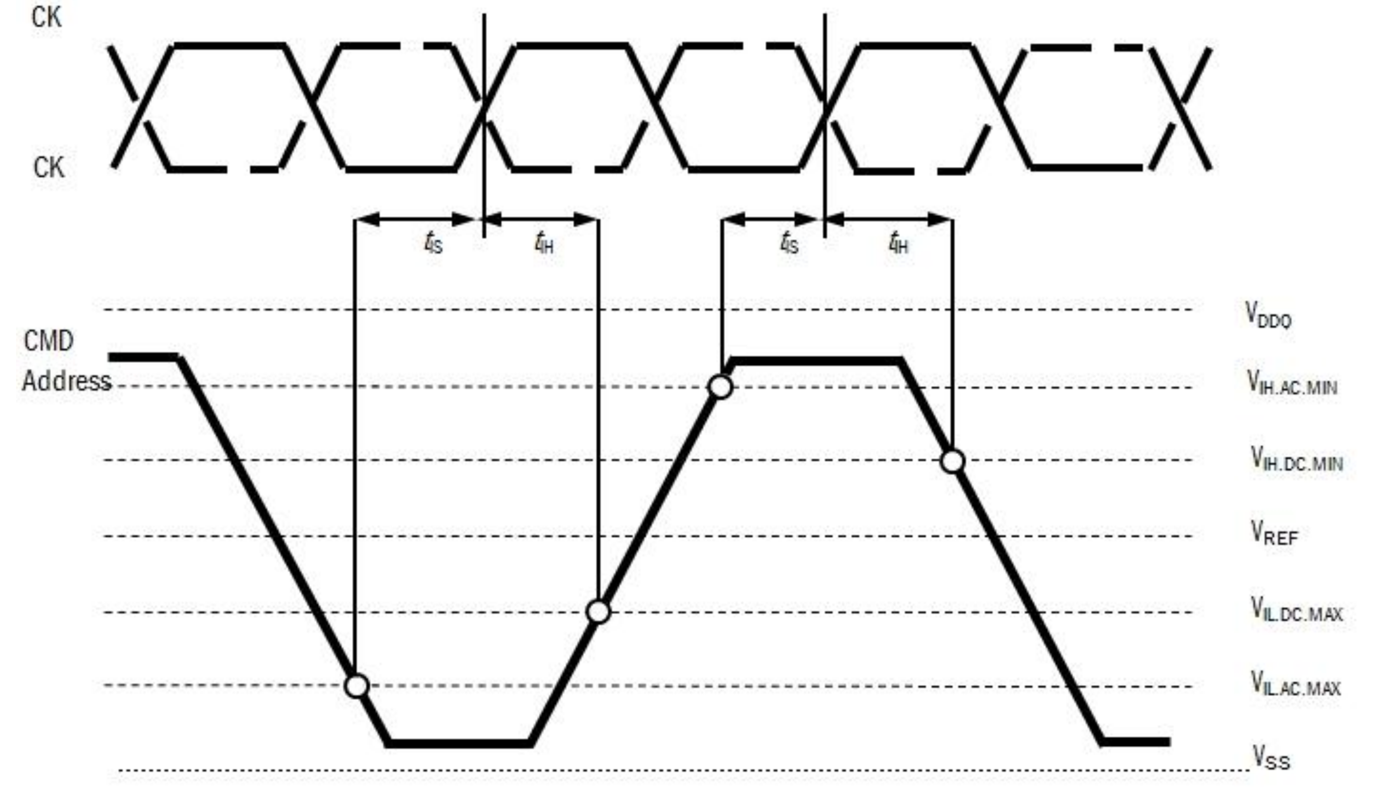


Figure 10 - Differential Input Waveform Timing - t_{IS} and t_{IH}



7.3 Jitter Definition and Clock Jitter Specification

Generally, jitter is defined as “the short-term variation of a signal with respect to its ideal position in time”. The following table provides an overview of the terminology.

Table 37 - Average Clock and Jitter Symbols and Definition

Symbol	Parameter	Description	Units
$t_{CK.AVG}$	Average clock period	$t_{CK.AVG}$ is calculated as the average clock period within any consecutive 200-cycle window: $tCK(avg) = \left[\sum_{j=1}^{N} tCK_j \right] / N$ N = 200	ps
$t_{JIT.PER}$	Clock-period jitter	$t_{JIT.PER}$ is defined as the largest deviation of any single t_{CK} from $t_{CK.AVG}$: $t_{JIT.PER}$ = Min/Max of $\{t_{CKi} - t_{CK.AVG}\}$ where i = 1 to 200 $t_{JIT.PER}$ defines the single-period jitter when the DLL is already locked. $t_{JIT.PER}$ is not guaranteed through final production testing.	ps
t_{JIT}(PER, LCK)	Clock-period jitter during DLL-locking period	t_{JIT}(PER,LCK) uses the same definition as $t_{JIT.PER}$, during the DLL-locking period only. t_{JIT}(PER,LCK) is not guaranteed through final production testing.	ps
$t_{JIT.CC}$	Cycle-to-cycle clock period jitter	$t_{JIT.CC}$ is defined as the absolute difference in clock period between two consecutive clock cycles: $t_{JIT.CC}$ = Max of ABS$\{t_{CKi+1} - t_{CKi}\}$ $t_{JIT.CC}$ defines the cycle - to - cycle jitter when the DLL is already locked. $t_{JIT.CC}$ is not guaranteed through final production testing.	ps
t_{JIT}(CC, LCK)	Cycle-to-cycle clock period jitter during DLL-locking period	t_{JIT}(CC,LCK) uses the same definition as $t_{JIT.CC}$ during the DLL-locking period only. t_{JIT}(CC,LCK) is not guaranteed through final production testing.	ps
$t_{ERR.2PER}$	Cumulative error across 2 cycles	$t_{ERR.2PER}$ is defined as the cumulative error across 2 consecutive cycles from $t_{CK.AVG}$: $tERR(nper) = \left[\sum_{j=1}^{i+n-1} tCK_j \right] - n \times tCK(avg)$ n = 2 for t_{ERR}(2per) where i = 1 to 200	ps

Symbol	Parameter	Description	Units
$t_{ERR.nPER}$	Cumulative error across n cycles	$t_{ERR.2PER}$ is defined as the cumulative error across n consecutive cycles from $t_{CK.AVG}$: $tERR(nper) = \left[\sum_{j=1}^{i+n-1} tCK_j\right] - n \times$ where, i = 1 to 200 and n = 3 for $t_{ERR.3PER}$ n = 4 for $t_{ERR.4PER}$ n = 5 for $t_{ERR.5PER}$ $6 \leq n \leq 10$ for $t_{ERR.6-10PER}$ $11 \leq n \leq 50$ for $t_{ERR.11-50PER}$	Ps
$t_{CH.AVG}$	Average high-pulse width	$t_{CH.AVG}$ is defined as the average high-pulse width, as calculated across any consecutive 200 high pulses: N=200 $tCH(avg) = \left[\sum_{j=1}^{N} tCH_j\right] / (N \times tCK(avg))$	$t_{CK.AVG}$
$t_{CL.AVG}$	Average low-pulse width	$t_{CL.AVG}$ is defined as the average low-pulse width, as calculated across any consecutive 200 low pulses: N=200 $tCL(avg) = \left[\sum_{j=1}^{N} tCL_j\right] / (N \times tCK(avg))$	$t_{CK.AVG}$
$t_{JIT.DUTY}$	Duty-cycle jitter	$t_{JIT.DUTY}$ = Min/Max of {$t_{JIT.CH}$, $t_{JIT.CL}$}, where: $t_{JIT.CH}$ is the largest deviation of any single t_{CH} from $t_{CH.AVG}$ $t_{JIT.CL}$ is the largest deviation of any single t_{CL} from $t_{CL.AVG}$ $t_{JIT.CH} = \{t_{CHi} - t_{CH.AVG} \times t_{CK.AVG}\}$ where i=1 to 200 $t_{JIT.CL} = \{t_{CLi} - t_{CL.AVG} \times t_{CK.AVG}\}$ where i=1 to 200	ps

The following parameters are specified per their average values however, it is understood that the following relationship between the average timing and the absolute instantaneous timing holds all the time.

Table 38 - Absolute Jitter Value Definitions

Symbol	Parameter	Min.	Max.	Unit
$t_{CK.ABS}$	Clock period	$t_{CK.AVG(Min)} + t_{JIT.PER(Min)}$	$t_{CK.AVG(Max)} + t_{JIT.PER(Max)}$	ps
$t_{CH.ABS}$	Clock high-pulse width	$t_{CH.AVG(Min)} \times t_{CK.AVG(Min)} + t_{JIT.DUTY(Min)}$	$t_{CH.AVG(Max)} \times t_{CK.AVG(Max)} + t_{JIT.DUTY(Max)}$	ps
$t_{CL.ABS}$	Clock low-pulse width	$t_{CL.AVG(Min)} \times t_{CK.AVG(Min)} + t_{JIT.DUTY(Min)}$	$t_{CL.AVG(Max)} \times t_{CK.AVG(Max)} + t_{JIT.DUTY(Max)}$	ps

Table 39 - Clock-Jitter Specifications for DDR2–800 /DDR2-1066

Symbol	Parameter	DDR2-800		DDR2-1066		Unit
		Min.	Max.	Min.	Max.	
$t_{CK.AVG}$	Average clock period nominal w/o jitter	2500	8000	1875	7500	ps
$t_{JIT.PER}$	Clock-period jitter	–100	100	-90	90	ps
$t_{JIT(PER,LCK)}$	Clock-period jitter during DLL locking period	–80	80	–80	80	ps
$t_{JIT.CC}$	Cycle-to-cycle clock-period jitter	–200	200	–180	180	ps
$t_{JIT(CC,LCK)}$	Cycle-to-cycle clock-period jitter during DLL-locking period	–160	160	–160	160	ps
$t_{ERR.2PER}$	Cumulative error across 2 cycles	–150	150	–132	132	ps
$t_{ERR.3PER}$	Cumulative error across 3 cycles	–175	175	–157	157	ps
$t_{ERR.4PER}$	Cumulative error across 4 cycles	–200	200	–175	175	ps
$t_{ERR.5PER}$	Cumulative error across 5 cycles	–200	200	–188	188	ps
$t_{ERR(6-10PER)}$	Cumulative error across n cycles with n = 6 .. 10, inclusive	–300	300	–250	250	ps
$t_{ERR(11-50PER)}$	Cumulative error across n cycles with n = 11 .. 50, inclusive	–450	450	–425	425	ps
$t_{CH.AVG}$	Average high-pulse width	0.48	0.52	0.48	0.52	$t_{CK.AVG}$
$t_{CL.AVG}$	Average low-pulse width	0.48	0.52	0.48	0.52	$t_{CK.AVG}$
$t_{JIT.DUTY}$	Duty-cycle jitter	–100	100	–75	75	ps

7.4 ODT AC Electrical Characteristics

This chapter describes the ODT AC electrical characteristics.

Table 40 - ODT AC Characteristics and Operating Conditions for DDR2-800 / DDR2-1066

Symbol	Parameter	DDR2-800		DDR2-1066		Unit	Note
		Min.	Max.	Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	2	2	n_{CK}	1
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	$t_{AC.MIN}$	$t_{AC.MAX}$ + 2.575 ns	ns	1 2
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	$t_{AC.MIN}$ + 2 ns	3 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1
t_{AOFD}	ODT turn-off delay	2.5	2.5	2.5	2.5	n_{CK}	1
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1 3
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$+ 1 ns	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$+ 1 ns	ns	1
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	–	4	–	n_{CK}	1
t_{AXPD}	ODT Power Down Exit Latency	8	–	11	–	n_{CK}	1

[1] New units, "$t_{CK.AVG}$" and "n_{CK}", are introduced in DDR2-800. Unit "$t_{CK.AVG}$" represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit "n_{CK}" represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, "t_{CK}" is used for both concepts. Example: t_{XP} = 2 [n_{CK}] means; if Power Down exit is registered at T_m, an Active command may be registered at T_m + 2, even if (T_m + 2 - T_m) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.

[2] ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-800 t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.

[3] ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-800, if $t_{CK(avg)}$ = 3 ns is assumed, t_{AOFD} is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

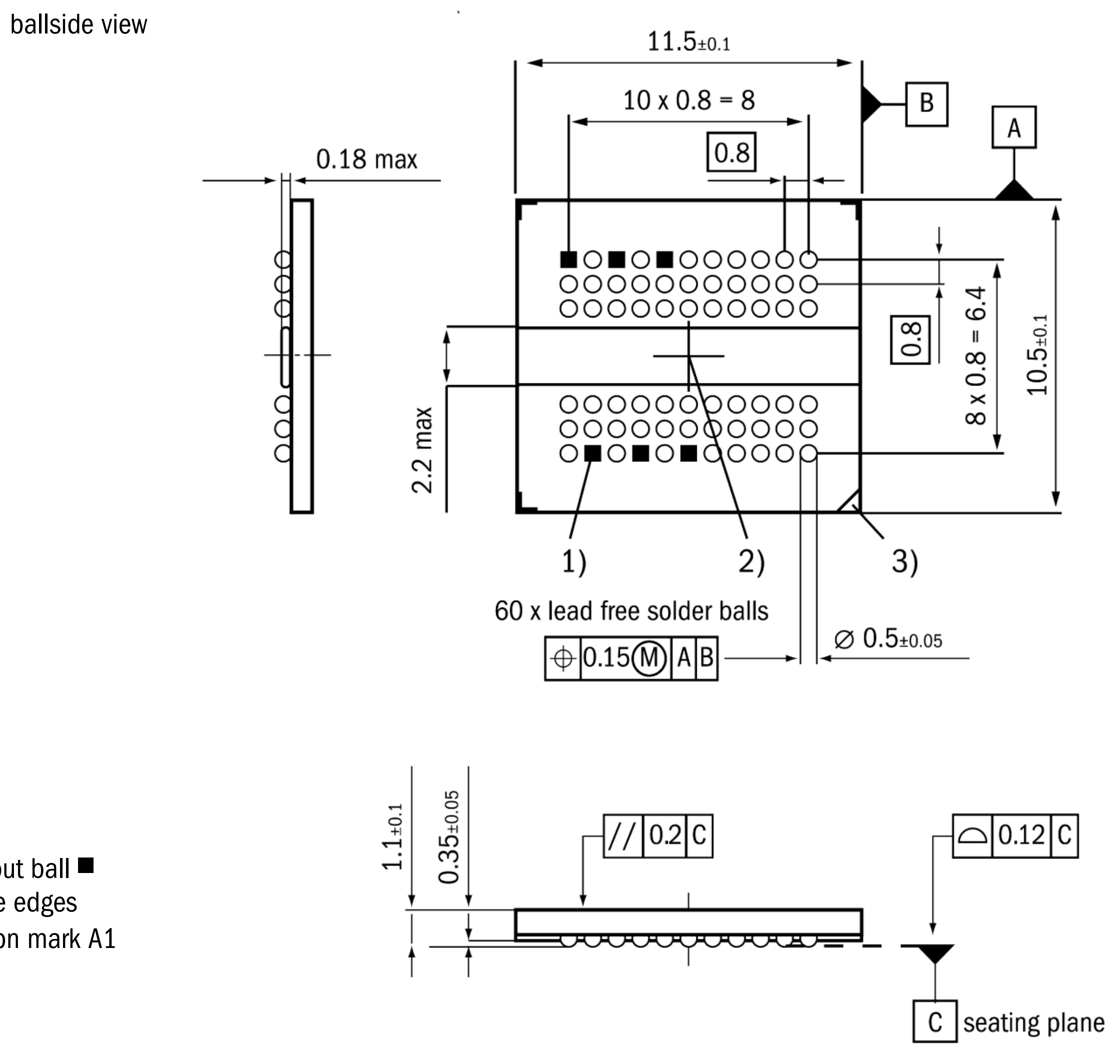
8 | Package Outline

This chapter contains the package dimension figures.

Notes

1. Drawing according to ISO 8015
2. Dimensions in mm
3. General tolerances +/- 0.15

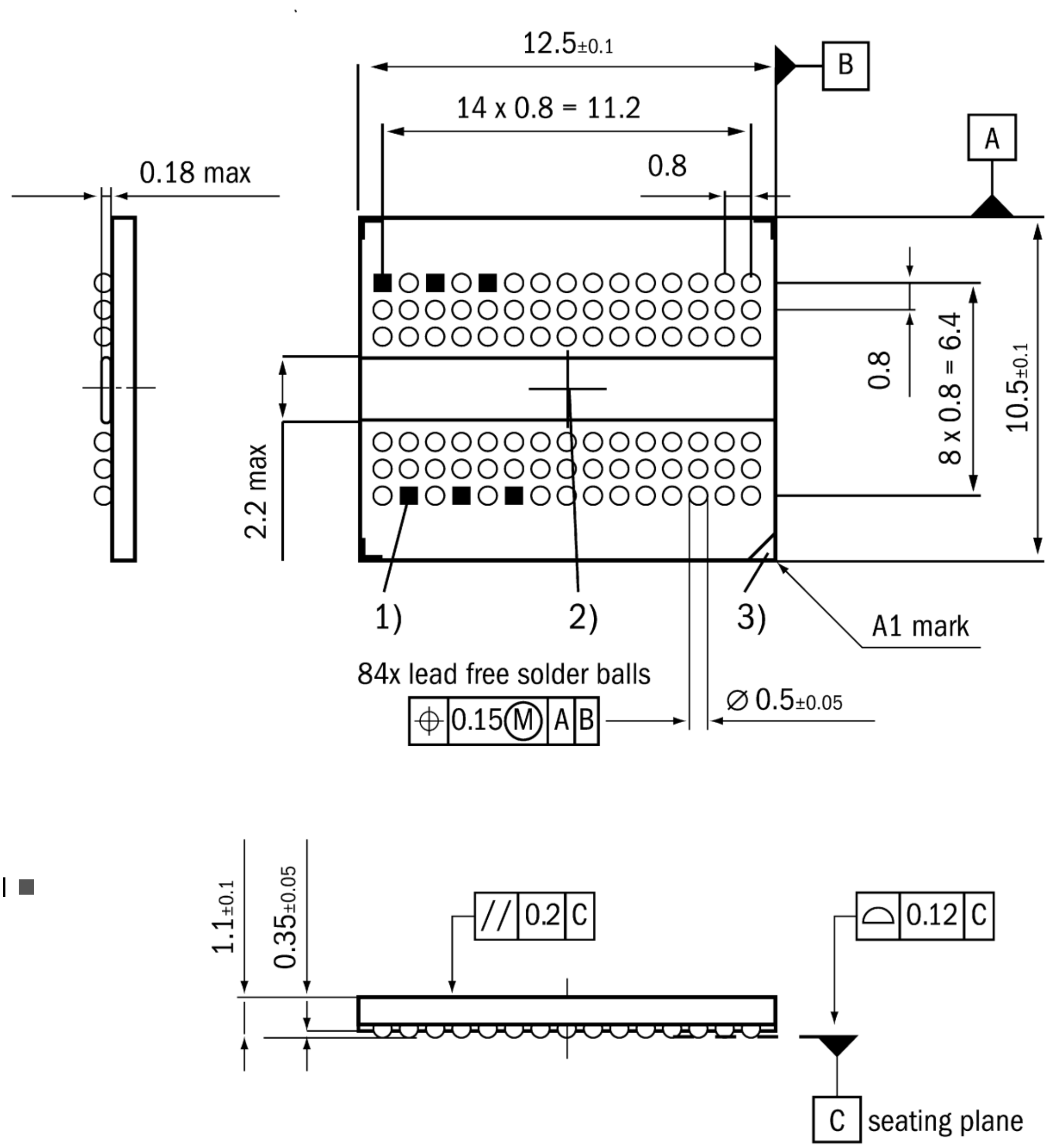
Figure 11 - Package Outline TFBGA-60



Lead free solder balls
(green solder balls)

1) Dummy pad without ball ■
2) Middle of package edges
3) Package orientation mark A1

Figure 12 - Package Outline TFBGA-84



Lead free solder balls
(green solder balls)

1) Dummy pad without ball ■
2) Middle of package edges
3) Package orientation mark A1

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