

MEM512M72D2MVD-25A1 4 Gigabyte (512M x 72 Bit)
MEM512M72D2MVD-3A1 4 Gigabyte (512M x 72 Bit)

Very-Low-Profile DDR2 SDRAM Registered Mini-DIMM memory module
RoHS Compliant Product

Memphis Electronic AG

Version: Rev. 1.1, MAR 2011

SPD values for Byte 28 and Byte 40 modified

Version: Rev. 1.0, OCT 2010

1.0 Initial release

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Features

- 244- Pin VLP Registered Mini Dual-In-Line Memory Module with Address and Command Parity
- Capacity: 4GB
- Maximum Data Transfer Rate MEM512M72D2MVD-3A1: 5.30 GB/Sec
Maximum Data Transfer Rate MEM512M72D2MVD-25A1: 6.40 GB/Sec
- JEDEC-Standard
- Power Supply: VDD, VDDQ = 1.8± 0.1 V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL): 4, 5 (Clock)
- Programmable Additive Latency (AL) : 0, 1, 2, 3 and 4 (Clock)
- Write Latency(WL) = Read Latency(RL) - 1
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- SSTL_18 Interface
- Gold Edge Contacts
- 100% RoHS-Compliant
- Very Low Profile Module Height: 18.2mm(0.72 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Speed	Memory Clock	Clock Cycles (CL-t _{RCD} -t _{RP})	Temperature Range	Module Type
MEM512M72D2MVD-25A1	PC2-6400 / DDR2-800	400MHz	5-5-5	0° to 95°C	4GB DDR2 Reg. Mini-DIMM
MEM512M72D2MVD-3A1	PC2-5300 / DDR2-667	333Mhz	5-5-5	0° to 95°C	4GB DDR2 Reg. Mini-DIMM

Note: The average refresh-interval must be reduced to 3.9µs (MAX) when TCASE exceeds +85°C

Table 2 - Performance Range

Speed	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
MEM512M72D2MVD-25A1	
PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=5)
PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)
PC2-4200 (DDR2-533)	266MHz (3.75ns@CL=4)
MEM512M72D2MVD-3A1	
PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)
PC2-4200 (DDR2-533)	266MHz (3.75ns@CL=4)

Table 3 - Memory Chip Information

Brand	Part No	Type.	ChipPacking
Memphis	MEM4G08D2DADG-25	4Gb DDP (256Mx8)x2	Lead Free

Table 4 - Addressing

Parameter	Value
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	4Gb DDP (256Mx8)x2
Column address	A[9, 0]
Module rank address	2 /S[1:0]
Number of devices	9

Table 5 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	123	VSS	62	A4	184	VDDQ
2	VSS	124	D4	63	VDDQ	185	A3
3	D0	125	D5	64	A2	186	A1
4	D1	126	VSS	65	VDD	187	VDD
5	VSS	127	DM0	66	VSS	188	CK0
6	$\overline{\text{DQS0}}$	128	NC	67	VSS	189	$\overline{\text{CK0}}$
7	DQS0	129	VSS	68	PAR_IN	190	VDD
8	VSS	130	D6	69	VDD	191	A0
9	D2	131	D7	70	A10	192	BA1
10	D3	132	VSS	71	BA0	193	VDD
11	VSS	133	D12	72	VDD	194	$\overline{\text{RAS}}$
12	D8	134	D13	73	$\overline{\text{WE}}$	195	VDDQ
13	D9	135	VSS	74	VDDQ	196	$\overline{\text{S0}}$
14	VSS	136	DM1	75	$\overline{\text{CAS}}$	197	VDDQ
15	$\overline{\text{DQS1}}$	137	NC	76	VDDQ	198	ODT0
16	DQS1	138	VSS	77	$\overline{\text{S1}}$	199	A13
17	VSS	139	NC	78	ODT1	200	VDD
18	$\overline{\text{RESET}}$	140	NC	79	VDDQ	201	NC
19	NC	141	VSS	80	NC	202	VSS
20	VSS	142	D14	81	VSS	203	D36
21	D10	143	D15	82	D32	204	D37
22	D11	144	VSS	83	D33	205	VSS
23	VSS	145	D20	84	VSS	206	DM4
24	D16	146	D21	85	$\overline{\text{DQS4}}$	207	NC
25	D17	147	VSS	86	DQS4	208	VSS
26	VSS	148	DM2	87	VSS	209	D38
27	$\overline{\text{DQS2}}$	149	NC	88	D34	210	D39
28	DQS2	150	VSS	89	D35	211	VSS
29	VSS	151	D22	90	VSS	212	D44
30	D18	152	D23	91	D40	213	D45
31	D19	153	VSS	92	D41	214	VSS
32	VSS	154	D28	93	VSS	215	DM5
33	D24	155	D29	94	$\overline{\text{DQS5}}$	216	NC
34	D25	156	VSS	95	DQS5	217	VSS
35	VSS	157	DM3	96	VSS	218	D46
36	$\overline{\text{DQS3}}$	158	NC	97	D42	219	D47
37	DQS3	159	VSS	98	D43	220	VSS
38	VSS	160	D30	99	VSS	221	D52
39	D26	161	D31	100	D48	222	D53
40	D27	162	VSS	101	D49	223	VSS
41	VSS	163	CB4	102	VSS	224	NC
42	CB0	164	CB5	103	SA2	225	NC
43	CB1	165	VSS	104	NC	226	VSS
44	VSS	166	DM8	105	VSS	227	DM6
45	$\overline{\text{DQS8}}$	167	NC	106	$\overline{\text{DQS6}}$	228	NC
46	DQS8	168	VSS	107	DQS6	229	VSS
47	VSS	169	CB6	108	VSS	230	D54
48	CB2	170	CB7	109	D50	231	D55
49	CB3	171	VSS	110	D51	232	VSS
50	VSS	172	NC	111	VSS	233	D60
51	NC	173	VDDQ	112	D56	234	D61
52	VDDQ	174	CKE1	113	D57	235	VSS
53	CKE0	175	VDD	114	VSS	236	DM7
54	VDD	176	NC	115	$\overline{\text{DQS7}}$	237	NC
55	BA2	177	A14	116	DQS7	238	VSS
56	$\overline{\text{ERR_OUT}}$	178	VDDQ	117	VSS	239	D62
57	VDDQ	179	A12	118	D58	240	D63
58	A11	180	A9	119	D59	241	VSS
59	A7	181	VDD	120	VSS	242	SDA
60	VDD	182	A8	121	SA0	243	SCL
61	A5	183	A6	122	SA1	244	VDDSPD

Table 6 - Pin Description

Pin Name	Description	Pin Name	Description
VDD*	SDRAM core power supply	VDDQ*	SDRAM I/O Driver power supply
VREF	SDRAM I/O reference supply	VSS	Power supply return (ground)
A0-A14	SDRAM address bus	BA0-BA2	SDRAM bank select
CK0	SDRAM clocks (positive line of differential pair)	/CK0	SDRAM clocks (negative line of differential pair)
/RAS	SDRAM row address strobe	/CAS	SDRAM column address strobe
/WE	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
/S0-/S1	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS7	SDRAM data strobes (positive line of differential pair)	/DQS0- /DQS7	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	DM0-DM7	SDRAM data masks/high data strobes
CB0-CB7	Data check bits Input/Output	SDA	EEPROM data line
SCL	EEPROM clock	VDDSPD	EEPROM positive power supply
SA0-SA2	EEPROM address input	/RESET	Register and PLL control pin
PAR_IN	Parity bit for the Address and Control Bus	/ERR_OUT	Parity error found in Address and Control pin
NC	Spare Pins (no connect)	-	-

*The VDD and VDDQ pins are tied common to a single power-plane on this design

Figure 1 - PCB Dimension 244 Pin DDR2 SDRAM Registered Mini-DIMM

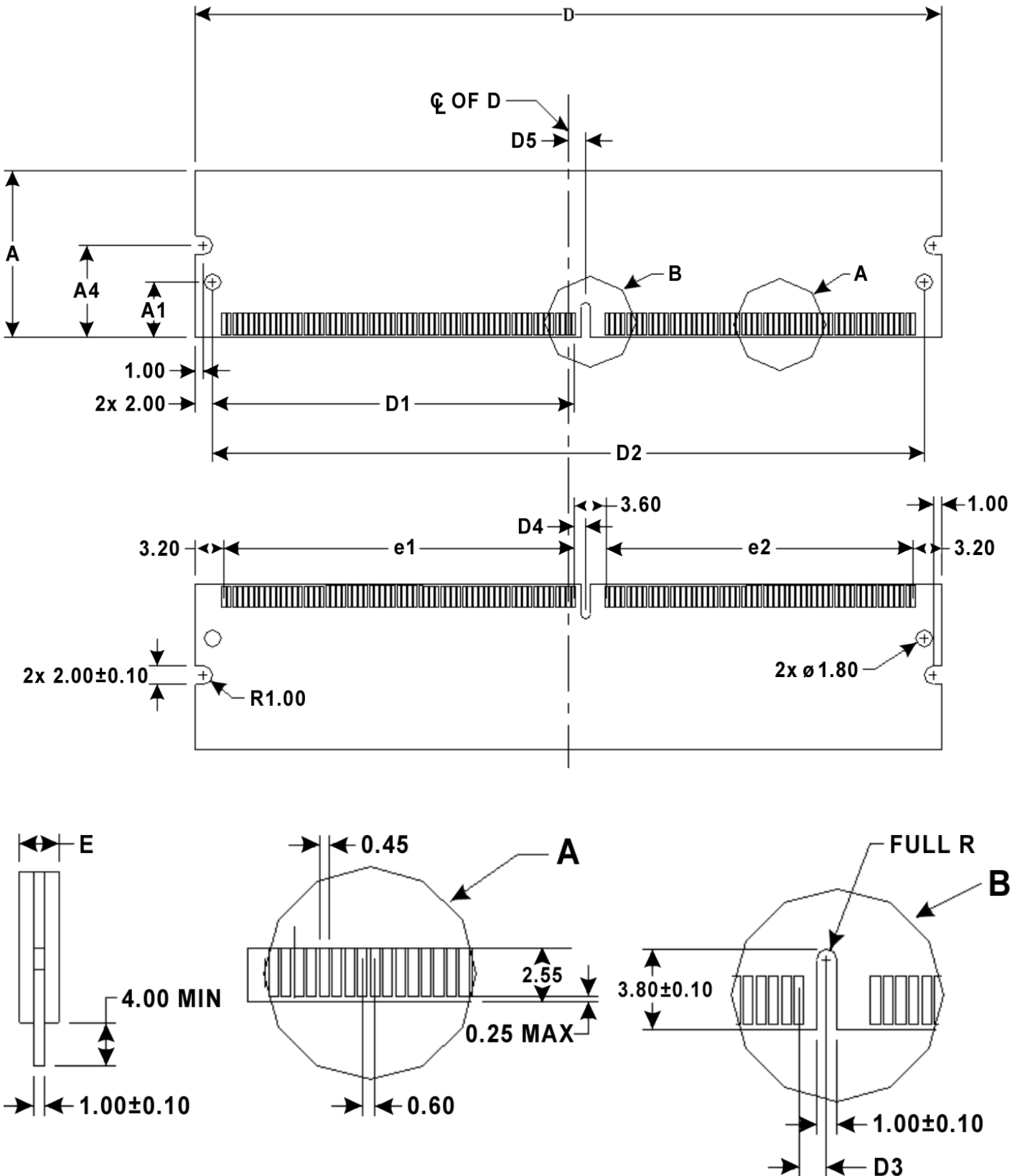


Table 7 - PCB Dimension

Symbol	MIN	NOM	MAX
A	18.05	18.2	18.35
A1	6.00 Basic		
A4	10.00 Basic		
D	81.85	82.00	82.15
D1	39.60 Basic		
D2	78.00 Basic		
D3	1.30 Basic		
D4	1.30 Basic		
D5	1.90 Basic		
E1	38.40 Basic		
E2	33.60 Basic		
E			3.80

Notes:

- Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances on all dimensions ± 0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 - Functional Block Diagram (Page 1 of 2)

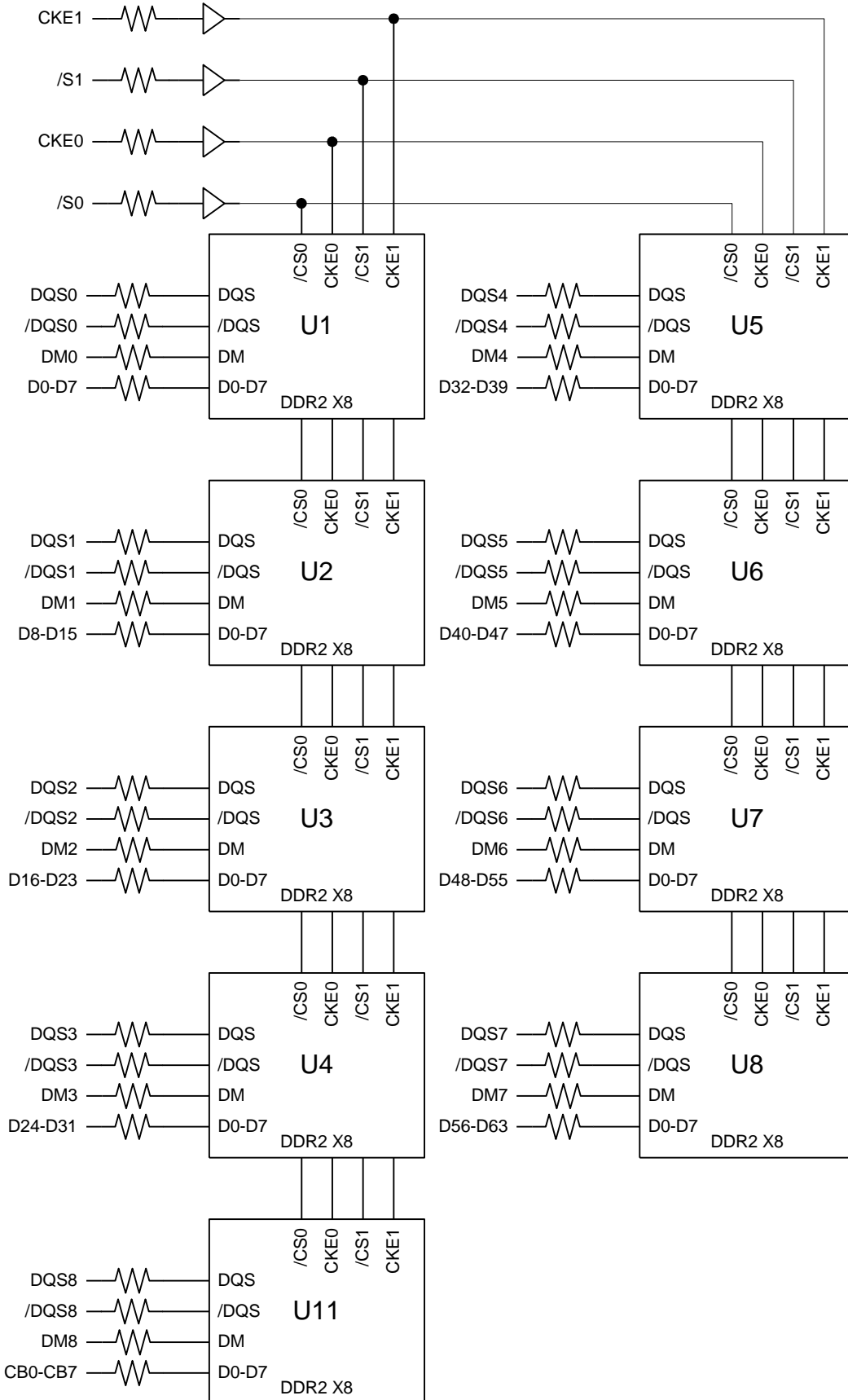
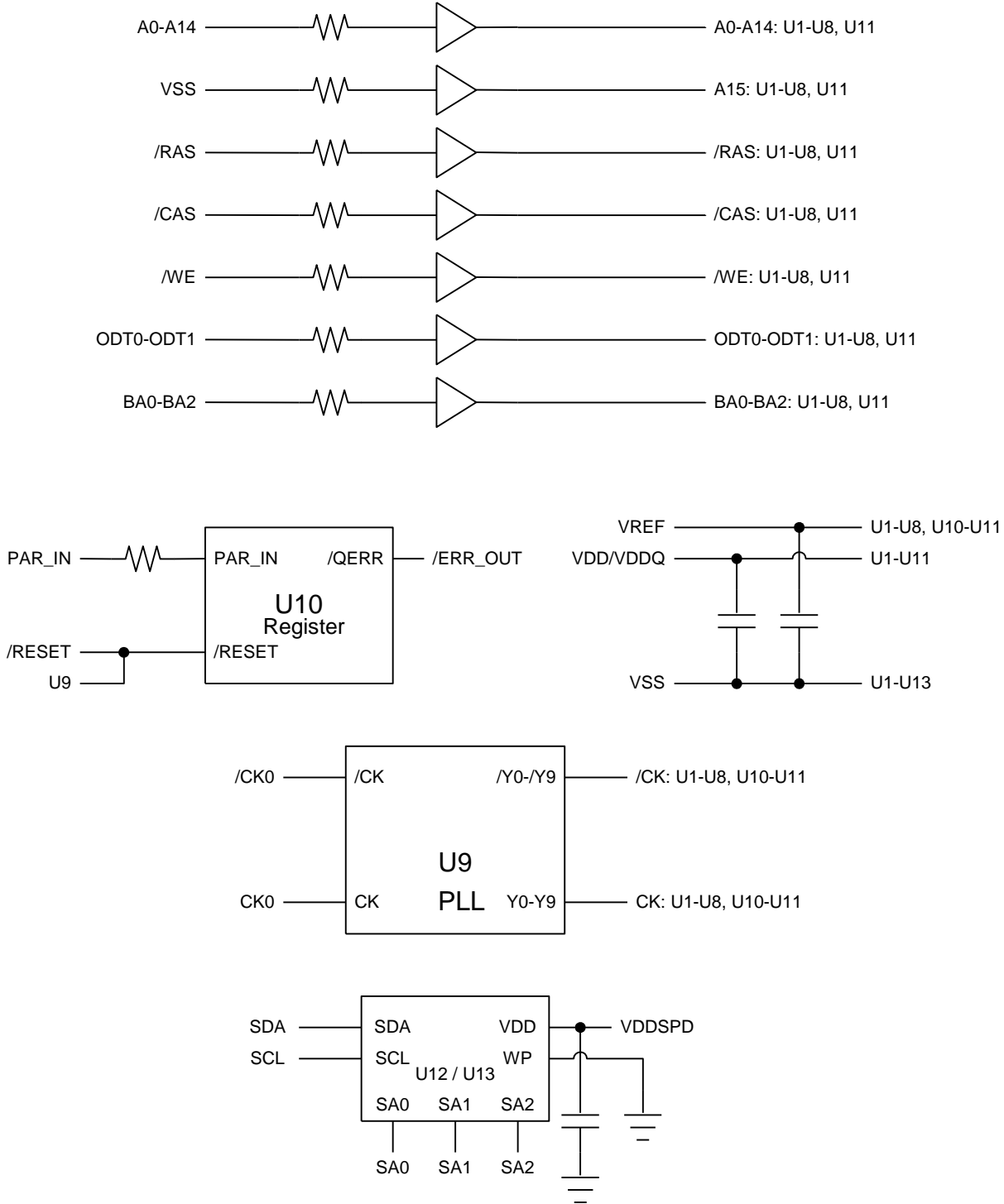


Figure 3 - Functional Block Diagram (Page 2 of 2)



Electrical Parameter

Table 8 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V _{DD} , pin relative to V _{SS}	V _{DD}	-1.0V ~ 2.3	V	1
Voltage on V _{DDQ} , pin relative to V _{SS}	V _{DDQ}	-0.5V ~ 2.3	V	1
Voltage on V _{DDL} , pin relative to V _{SS}	V _{DDL}	-0.5V ~ 2.3	V	1
Voltage on any pins relative to V _{SS}	V _{IN} , V _{OUT}	-0.5V ~ 2.3	V	1
Storage temperature	T _{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Ambient)	T _{OPER}	0 ~ 95	°C	3,4

Notes:

- 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- 3 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
- 4 At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (tREFI=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

Table 9 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V _{DD}	1.7	1.8	1.9	V	
Supply voltage for DLL	V _{DDL}				V	4
Supply voltage for Output	V _{DDQ}				V	4
Input reference voltage	V _{REF}	0.49* V _{DDQ}	0.50* V _{DDQ}	0.51* V _{DDQ}	mV	1,2
Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	3
DC input logic high voltage	V _{IH}	V _{REF} +0.125	-	V _{DDQ} +0.3	V	
DC input logic low voltage	V _{IL}	-0.3	-	V _{REF} -0.125	V	

Notes:

- 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
- 2 Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
- 3 VTT of transmitting device must track VREF of receiving device.
- 4 AC parameters are measured with VDD, VDDQ and VDDL tied together.

Table 10 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating precharge current; one bank active, tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD0}	756	mA	1, 2
Operating read-precharge current; one bank active, I _{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	I _{DD1}	828	mA	1, 2
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	I _{DD2P}	216	mA	1, 3
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	I _{DD2Q}	810	mA	1, 3
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD2N}	900	mA	1,3
Active power-down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	288	mA	1, 3
	Slow PDN Exit MRS(12) = 1mA	288	mA	1, 3
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD3N}	990	mA	1, 3
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD4W}	1188	mA	1, 2
Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	I _{DD4R}	1323	mA	1, 2
Burst auto refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD5}	2880	mA	1, 3
Self refresh current; CK and CK\ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	I _{DD6}	216	mA	1, 3
Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(IDD), tRC = tRC(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	I _{DD7}	1908	mA	1, 2

Notes:

- ¹ Value shown for DDR2 SDRAM only and are computed from values specified in the 2Gbit component data sheet.
- ² Value calculated as one module rank in this operating condition. All other module ranks in IDD2P (CKE LOW) mode.
- ³ Value calculated reflects all module ranks in this operating condition.

Table 11 - AC Timing Parameter and Operating Conditions

Parameter / Condition	Symbol	Min		Max		Units
		MEM512M72 D2MVD-25A1	MEM512M72 D2MVD-3A1	MEM512M72 D2MVD 25A1	MEM512M72 D2MVD-3A1	
DQ output access time from CK/CK	tAC	-400	-450	+400	+450	ps
DQS output access time from CK/CK	tDQSCK	-350	-400	+350	+400	ps
CK high-level width	tCH	0.48	0.48	0.52	0.52	tCK
CK low-level width	tCL	0.48	0.48	0.52	0.52	tCK
CK half period	tHP	Min(tCL, tCH)	Min(tCL, Tch)	-	-	ps
DQ and DM input hold time	tDH	125	175	-	-	ps
RAS to CAS delay	tRCD	12.5	15	-	-	ns
Row precharge time	tRP	12.5	15	-	-	ns
Row cycle time	tRC	57.5	60	-	-	ns
Row active time	tRAS	45	45	70000	70000	ns
Clock cycle time	tCK (CL=3)	5	5	8	8	ns
	tCK (CL=4)	3.75	3.75	8	8	
	tCK (CL=5)	2.5	3	8	8	
DQ and DM input setup time	tDS	50	100	-	-	ps
Control & Address input pulse width for each input	tIPW	0.6	0.6	-	-	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	0.35	-	-	tCK
Data-out high-impedance time from CK/CK	tHZ	-	-	tAC max	tAC max	ps
DQ low-impedance time from CK/CK	tLZ	2*tAC min	2*tAC min	tAC max	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	-	200	240	ps
DQ hold skew factor	tQHS	-	-	300	340	ps
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	tHP-tQHS	-	-	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	-0.25	0.25	0.25	tCK
DQS input high pulse width	tDQSH	0.35	0.35	-	-	tCK
DQS input low pulse width	tDQSL	0.35	0.35	-	-	tCK
DQS falling edge to CK setup time	tDSS	0.2	0.2	-	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	0.2	-	-	tCK
Mode register set command cycle time	tMRD	2	2	-	-	tCK
Write postamble	tWPST	0.4	0.4	0.6	0.6	tCK
Write preamble	tWPRE	0.35	0.35	-	-	tCK
Address and control input hold time	tIH	250	275	-	-	ps
Address and control input setup time	tIS	175	200	-	-	ps
Read preamble	tRPRE	0.9	0.9	1.1	1.1	tCK
Read postamble	tRPST	0.4	0.4	0.6	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	7.5	-	-	ns
Four Activate Window for 1KB page size products	tFAW	35	37.5	-	-	ns
CAS to CAS command delay	tCCD	2	2	-	-	tCK
Write recovery time	tWR	15	15	-	-	ns
Auto precharge write recovery + precharge time	tDAL	WR+tRP	WR+tRP	-	-	tCK
Internal write to read command delay	tWTR	7.5	7.5	-	-	ns
Internal read to precharge command delay	tRTP	7.5	7.5	-	-	ns
Exit self refresh to a non-read command	tXSNR	tRFC+10	tRFC+10	-	-	ns
Exit self refresh to a read command	tXSRD	200	200	-	-	tCK
Exit precharge power down to any non read command	tXP	2	2	-	-	tCK
Exit active power down to read command	tXARD	2	2	-	-	tCK
Exit active power down to read command (slow exit, lower power)	tXARDS	8-AL	7-AL	-	-	tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3	3	-	-	tCK

Parameter / Condition	Symbol	Min		Max		Units
		MEM512M72 D2MVD-25A1	MEM512M72 D2MVD-3A1	MEM512M72 D2MVD 25A1	MEM512M72 D2MVD-3A1	
ODT turn-on delay	tAOND	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(min)	tAC(max)+ 0.7	tAC(max)+ 0.7	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	tAC(min)+2	2tCK+ tAC(max)+1	2tCK+ tAC(max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(min)	tAC(max)+ 0.6	tAC(max)+ 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	tAC(min)+2	2.5tCK+ tAC(max)+1	2.5tCK+ tAC(max)+1	ns
ODT to power down entry latency	tANPD	3	3	-	-	tCK
ODT power down exit latency	tAXPD	8	8	-	-	tCK
OCD drive mode output delay	tOIT	0	0	12	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	tIS+tCK+tIH	-	-	ns

Table 12 - SPD Information

Byte NO.	Description	Note		Hex	
		MEM512M72D2MVD -25A1	MEM512M72D2MVD -3A1	-25A1	-3A1
0	Number of serial PD Bytes written during module production	128 bytes	128 bytes	80	80
1	Total number of bytes in serial PD device	256 bytes	256 bytes	08	08
2	Fundamental memory type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of row addresses on this assembly	15	15	0F	0F
4	Number of column addresses on this assembly	10	10	0A	0A
5	Number of module rows on this assembly	2Rows less than 25.4mm	2Rows less than 25.4mm	01	01
6	Data width of this assembly	X72	X72	48	48
7	Reserved	-	-	00	00
8	Voltage interface level of this assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM cycle time at maximum supported CAS Latency (CL), CL=X	2.5ns	3.0ns	25	30
10	DDR2 SDRAM access time from clock at CL=X	0.4ns	0.45ns	40	45
11	DIMM configuration type (address & command parity, data parity or ECC)	ECC with Addr and Cmd Parity	ECC with Addr and Cmd Parity	06	06
12	Refresh rate/type	7.8us, self refresh	7.8us, self refresh	82	82
13	Primary DDR2 SDRAM width	x8	x8	08	08
14	Error checking DDR2 SDRAM data width	x8	x8	08	08
15	Reserved	-	-	00	00
16	DDR2 SDRAM device attributes: Burst lengths supported	4,8	4,8	0C	0C
17	DDR2 SDRAM device attributes: number of banks on each DDR2 SDRAM device	8 banks	8 banks	08	08
18	DDR2 SDRAM device attributes: CAS Latency	5, 4	5,4	30	30
19	DIMM mechanical characteristics	-	-	00	00
20	DIMM type information	Mini-RDIMM(82.0mm)	Mini-RDIMM(82.0mm)	10	10
21	DDR2 SDRAM module attributes	1 PLL and 1 Register	1 PLL and 1 Register	04	04
22	DDR2 SDRAM device attributes: General	Support weak driver	Support weak driver	03	03
23	Minimum clock cycle time at CL=X-1	and 50 ohm ODT	and 50 ohm ODT	3D	3D
24	Maximum data access time (tAC) from clock at CL=X-1	3.75ns	3.75ns	50	50
25	Minimum clock cycle time at CL=X-2	-	-	00	00
26	Maximum data access time (tAC) from clock at CL=X-2	-	-	00	00
27	Minimum row precharge time (tRP)	12.5ns	15.0ns	32	3C
28	Minimum row active to row active delay (tRRD)	7.5ns	7.5ns	1E	1E
29	Minimum RAS to CAS delay (tRCD)	12.5ns	15.0ns	32	3C
30	Minimum active to precharge time (tRAS)	45 ns	45 ns	2D	2D
31	Module rank density	2GB	2GB	02	02
32	Address and command input setup time before clock (tIS)	0.17ns	0.2ns	17	20
33	Address and command input hold time after clock (tIH)	0.25ns	0.27ns	25	27
34	Data input setup time before strobe (tDS)	0.05ns	0.1ns	05	10
35	Data input hold time after strobe (tDH)	0.12ns	0.17ns	12	17
36	Write recovery time (tWR)			3C	3C
37	Internal write to read command delay (tWTR)	7.5ns	7.5ns	1E	1E
38	Internal read to precharge command delay (tRTP)			1E	1E
39	Memory analysis probe characteristics	-	-	00	00

Byte NO.	Description	Note		Hex	
		MEM512M72D2MVD -25A1	MEM512M72D2MVD -3A1	- 25A1	-3A1
40	Extension of Byte 41 tRC and Byte 42 tRFC	tRC=57.5ns, tRFC=195ns	-	30	00
41	DDR2 SDRAM device minimum active to active/ auto-refresh Time (tRC)	57ns	60ns	39	3C
42	DDR2 SDRAM device minimum auto-refresh to active/auto-refresh command period (tRFC)	195ns	195ns	C3	C3
43	DDR2 SDRAM device maximum device cycle time (tCKmax)	8ns	8ns	80	80
44	DDR2 SDRAM device maximum skew between DQS and DQ signals (tDQSQ)	0.20ns	0.24ns	14	18
45	DDR2 SDRAM device maximum read data hold skew factor (tQHS)	0.30ns	0.34ns	1E	22
46	PLL relock time	15us	15us	0F	0F
47-48	DT in SPD	-	-	00	00
49	High temperature self-refresh rate support indication	-	-	00	00
50-61	IDD in SPD	-	-	00	00
62	SPD Data revision code	Rev 1.1	Rev 1.1	11	11
63	Checksum for bytes 0-62			26	7A
64-71	Manufacturer's JEDEC ID code	Manufacture's data	Manufacture's data		
72	Module manufacturing location	Manufacture's data	Manufacture's data		
73-90	Module part information	Manufacture's data	Manufacture's data		
91-92	Module revision code (For PCB& component)			0000	0000
93-94	Module manufacturing date	Manufacture's data	Manufacture's data		
95-98	Module serial number	Manufacture's data	Manufacture's data		
99-127	Manufacturer's specific data	Manufacture's data	Manufacture's data		
128-253	Open for customer use	-	-	00	00
254-255	Open for customer use	Manufacture's data	Manufacture's data	00	

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