

MEM512M72D2RVD-25A1 4GByte (512M x 72 Bit)

MEM512M72D2RVD-3A1 4GByte (512M x 72 Bit)

DDR2 VLP Registered Buffered DIMM
RoHS Compliant Product

Memphis Electronic AG

Version: Rev. 1.1, MAR 2011

SPD values for Byte 28 and Byte 40 modified

Version: Rev. 1.0, OCT 2010

1.0 Initial release

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Features

- 240-Pin VLP Registered Dual-In-Line Memory Module with Address and Command Parity
- Capacity: 4GB
- Maximum Data Transfer Rate MEM512M72D2RVD-25A1: 6.40 GB/Sec
Maximum Data Transfer Rate MEM512M72D2RVD-3A1: 5.30 GB/Sec
- JEDEC-Standard
- Power Supply: VDD, VDDQ = 1.8± 0.1 V
- Bi-directional Differential Data-Strobe (Single-ended data-strobe is an optional feature)
- 72 Bit Data Bus Width with ECC
- Programmable CAS Latency (CL): 4, 5 (Clock)
- Programmable Additive Latency (AL) : 0, 1, 2, 3 and 4 (Clock)
- Write Latency (WL) = Read Latency (RL) - 1
- Posted /CAS
- On-Die Termination (ODT)
- Off-Chip Driver (OCD) Impedance Adjustment
- Burst Type (Sequential & Interleave)
- Burst Length: 4, 8
- Refresh Mode: Auto and Self
- 8192 Refresh Cycles / 64ms
- Serial Presence Detect (SPD) with EEPROM
- SSTL_18 Interface
- Gold Edge Contacts
- 100% RoHS-Compliant
- Standard Module Height: 18.2mm (0.72 inch)

Table 1 - Ordering Information for RoHS Compliant Product

Part Number	Max. Speed	Memory Clock	Clock Cycles (CL-t _{RCD} -t _{RP})	Temperature Range	Module Type
MEM512M72D2RVD-25A1	PC2-6400	400MHz	5-5-5	0 to 95°C	4GB DDR2 RDIMM
MEM512M72D2RVD-3A1	PC2-5300	333MHz	5-5-5	0 to 95°C	4GB DDR2 RDIMM

Table 2 - Performance Range

Speed	Max Clock Frequency (min. Clock Cycle time @ min. CAS Latency)
MEM512M72D2RVD-25A1	
PC2-6400 (DDR2-800)	400MHz (2.5ns@CL=5)
PC2-4200 (DDR2-533)	266MHz (3.75ns@CL=4)
MEM512M72D2RVD-3A1	
PC2-5300 (DDR2-667)	333MHz (3.0ns@CL=5)
PC2-4200 (DDR2-533)	266MHz (3.75ns@CL=4)

Table 3 - Memory Chip Information

Brand	Part No	Type.	Chip Packing
Memphis	MEM2G08D2DABG-25	256Mx8	Lead Free

Table 4 - Addressing

Parameter	4GB
Refresh count	8K
Row address	32K A[14:0]
Device bank address	8 BA[2:0]
Device configuration	2Gb (256Mx8)
Column address	1K A[9:0]
Module rank address	2 /S[1:0]
Number of devices	18

Table 5 - Pin Assignment

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	121	VSS	61	A4	181	VDDQ
2	VSS	122	D4	62	VDDQ	182	A3
3	D0	123	D5	63	A2	183	A1
4	D1	124	VSS	64	VDD	184	VDD
5	VSS	125	$\overline{DQS9}$	65	VSS	185	CK0
6	$\overline{DQS0}$	126	DQS9	66	VSS	186	$\overline{CQ0}$
7	DQS0	127	VSS	67	VDD	187	VDD
8	VSS	128	D6	68	PAR_IN	188	A0
9	D2	129	D7	69	VDD	189	VDD
10	D3	130	VSS	70	A10/AP	190	BA1
11	VSS	131	D12	71	BA0	191	VDDQ
12	D8	132	D13	72	VDDQ	192	\overline{RAS}
13	D9	133	VSS	73	\overline{WE}	193	\overline{SA}
14	VSS	134	DQS10	74	\overline{CAS}	194	VDDQ
15	$\overline{DQS1}$	135	$\overline{DQS10}$	75	VDDQ	195	ODT0
16	DQS1	136	VSS	76	$\overline{S1}$	196	A13
17	VSS	137	NC	77	ODT1	197	VDD
18	\overline{RESET}	138	NC	78	VDDQ	198	VSS
19	NC	139	VSS	79	VSS	199	D36
20	VSS	140	D14	80	D32	200	D37
21	D10	141	D15	81	D33	201	VSS
22	D11	142	VSS	82	VSS	202	DQS13
23	VSS	143	D20	83	$\overline{DQS4}$	203	$\overline{DQS13}$
24	D16	144	D21	84	DQS4	204	VSS
25	D17	145	VSS	85	VSS	205	D38
26	VSS	146	DQS11	86	D34	206	D39
27	$\overline{DQS2}$	147	$\overline{DQS11}$	87	D35	207	VSS
28	DQS2	148	VSS	88	VSS	208	D44
29	VSS	149	D22	89	D40	209	D45
30	D18	150	D23	90	D41	210	VSS
31	D19	151	VSS	91	VSS	211	DQS14
32	VSS	152	D28	92	$\overline{DQS5}$	212	$\overline{DQS14}$
33	D24	153	D29	93	DQS5	213	VSS
34	D25	154	VSS	94	VSS	214	D46
35	VSS	155	DQS12	95	D42	215	D47
36	$\overline{DQS3}$	156	$\overline{DQS12}$	96	D43	216	VSS
37	DQS3	157	VSS	97	VSS	217	D52
38	VSS	158	D30	98	D48	218	D53
39	D26	159	D31	99	D49	219	VSS
40	D27	160	VSS	100	VSS	220	NC
41	VSS	161	CB4	101	SA2	221	NC
42	CB0	162	CB5	102	NC	222	VSS
43	CB1	163	VSS	103	VSS	223	DQS15
44	VSS	164	DQS17	104	$\overline{DQS6}$	224	$\overline{DQS15}$
45	$\overline{DQS8}$	165	$\overline{DQS17}$	105	DQS6	225	VSS
46	DQS8	166	VSS	106	VSS	226	D54
47	VSS	167	CB6	107	D50	227	D55
48	CB2	168	CB7	108	D51	228	VSS
49	CB3	169	VSS	109	VSS	229	D60
50	VSS	170	VDDQ	110	D56	230	D61
51	VDDQ	171	CKE1	111	D57	231	VSS
52	CKE0	172	VDD	112	VSS	232	DQS16
53	VDD	173	NC	113	$\overline{DQS7}$	233	$\overline{DQS16}$
54	BA2	174	A14	114	DQS7	234	VSS
55	$\overline{ERR_OUT}$	175	VDDQ	115	VSS	235	D62
56	VDDQ	176	A12	116	D58	236	D63
57	A11	177	A9	117	D59	237	VSS
58	A7	178	VDD	118	VSS	238	VDDSPD
59	VDD	179	A8	119	SDA	239	SA0
60	A5	180	A6	120	SCL	240	SA1

Table 6 - Pin Description

Pin Name	Description	Pin Name	Description
VDD*	SDRAM core power supply	VDDQ*	SDRAM I/O Driver power supply
VREF	SDRAM I/O reference supply	VSS	Power supply return (ground)
A0-A14	SDRAM address bus	BA0-BA2	SDRAM bank addresses
CK0	SDRAM clocks (positive line of differential pair)	$\overline{\text{CK0}}$	SDRAM clocks (negative line of differential pair)
$\overline{\text{RAS}}$	SDRAM row address strobe	$\overline{\text{CAS}}$	SDRAM column address strobe
$\overline{\text{WE}}$	SDRAM write enable	CKE0-CKE1	SDRAM clock enable lines
$\overline{\text{S0-S1}}$	DIMM Rank Select Lines	ODT0-ODT1	On-die termination control lines
DQS0-DQS17	SDRAM data strobes (positive line of differential pair)	$\overline{\text{DQS0 - DQS17}}$	SDRAM data strobes (negative line of differential pair)
D0-D63	DIMM memory data bus	CB0-CB7	Data check bits Input/Output
SCL	EEPROM clock	SDA	EEPROM data line
SA0 - SA2	EEPROM address input	VDDSPD	EEPROM positive power supply
PAR_IN	Parity bit for the address and control bus	$\overline{\text{ERR_OUT}}$	Parity error found in the address and control bus
NC	Spare Pins (no connect)	$\overline{\text{RESET}}$	Register and PLL control pin

*The VDD and VDDQ pins are tied common to a single power-plane on these designs.

Figure 1 - Module Dimension 240 Pin DDR2 SDRAM Registered DIMM

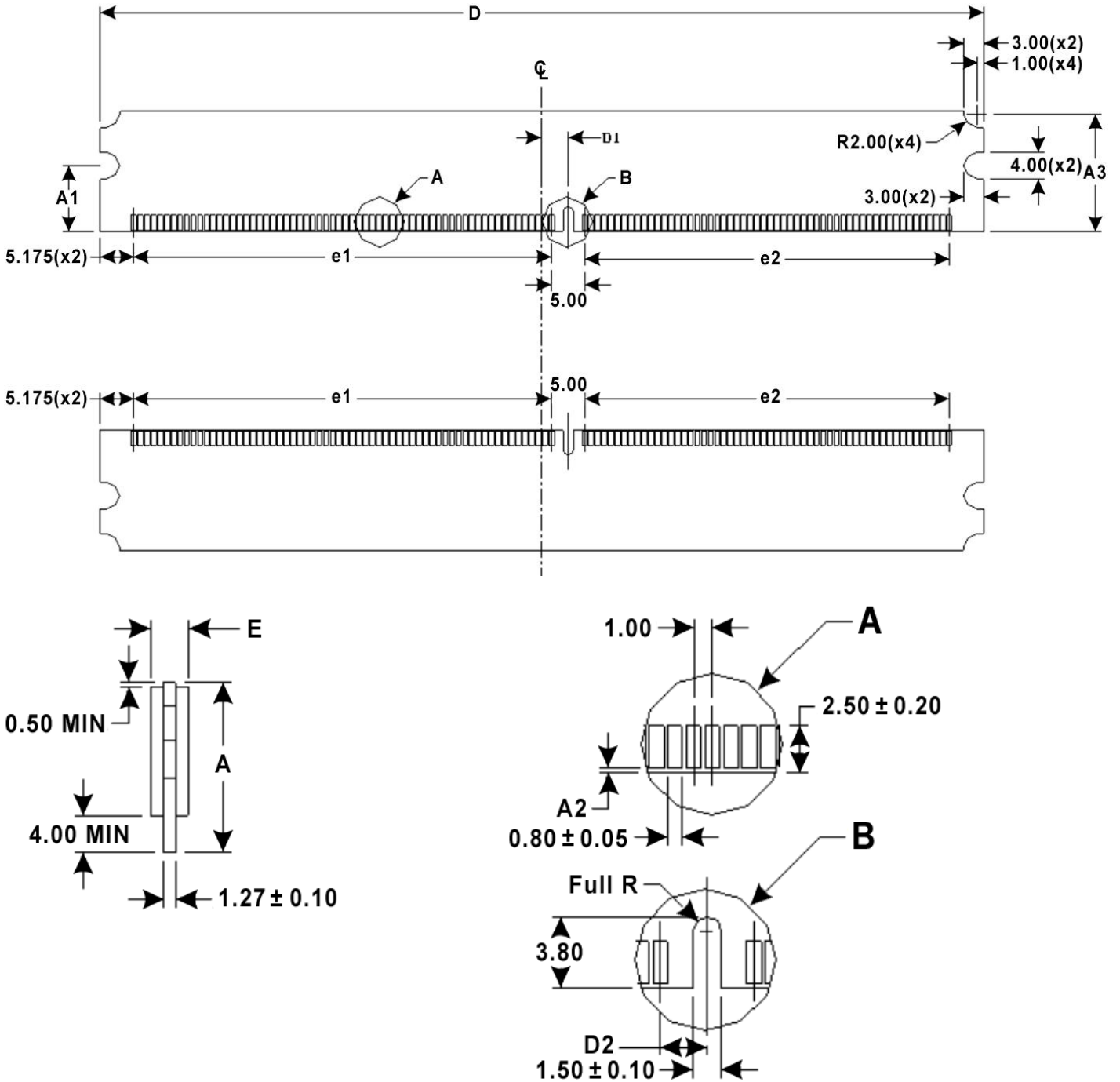


Table 7 - PCB Dimension

Symbol	MIN	NOM	MAX
A	18.15	18.30	18.80
A1	10.00 Basic		
A2	0.05	0.20	0.35
A3	17.80 Basic		
D	133.20	133.35	133.50
D1	4.00 Basic		
D2	2.50 Basic		
e1	63.00 Basic		
e2	55.00 Basic		
E			2.70

Notes:

- Dimensioning and tolerancing conform to ASME Y14.5M-1994.
- Tolerances for all dimensions ± 0.15 unless otherwise specified.
- All dimensions are in millimeters.

Figure 2 - Functional Block Diagram (Page 1 of 4)

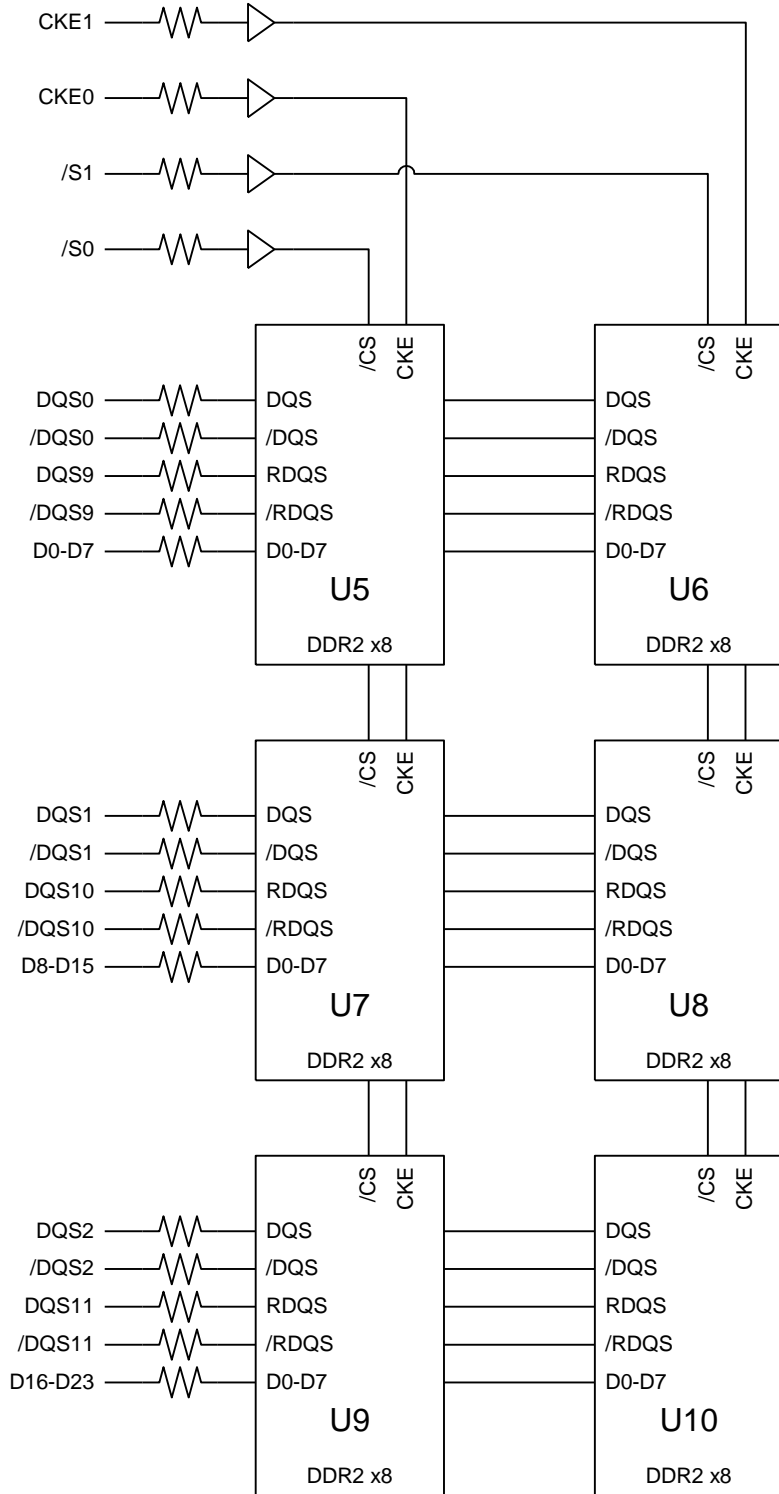


Figure 3 - Functional Block Diagram (Page 2 of 4)

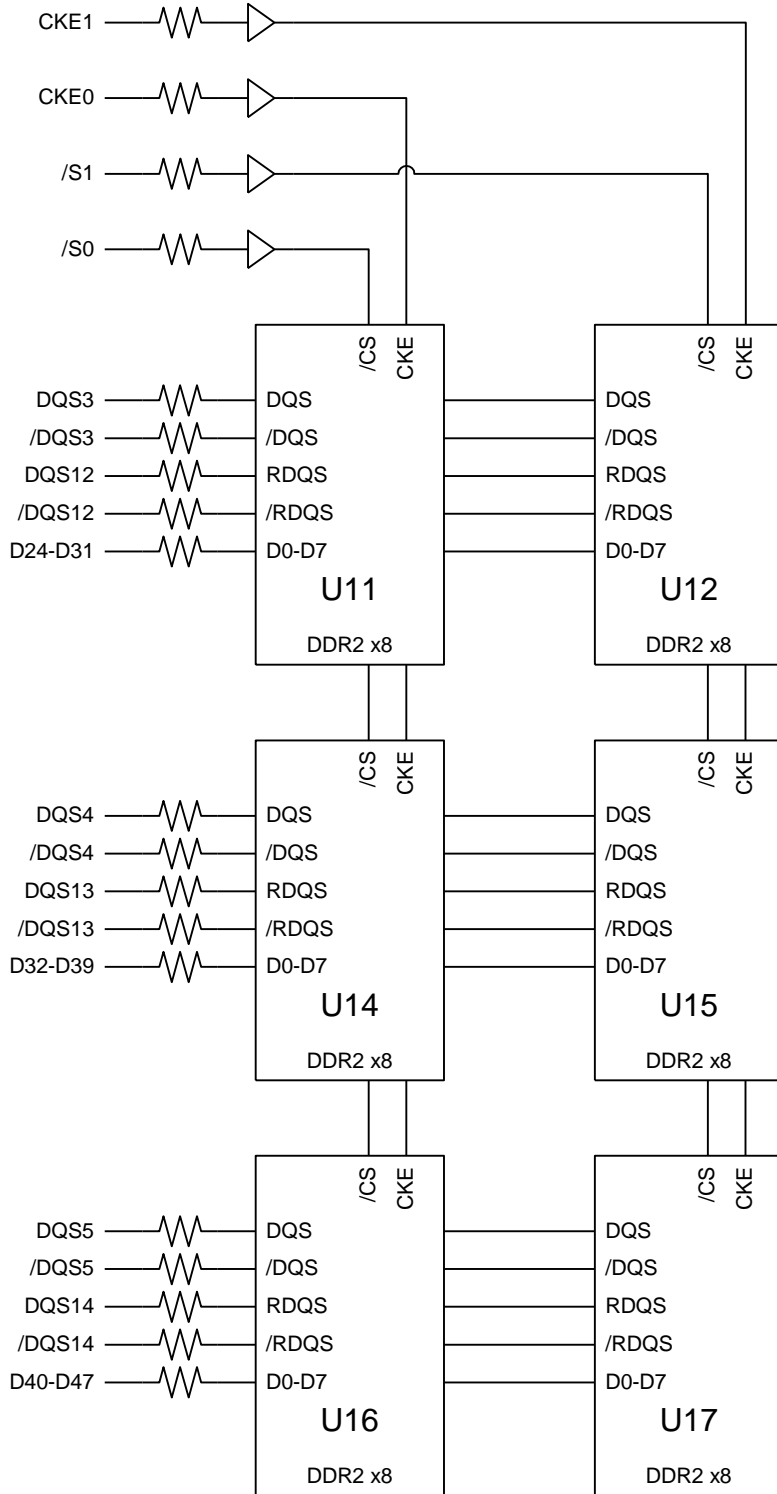


Figure 4 - Functional Block Diagram (Page 3 of 4)

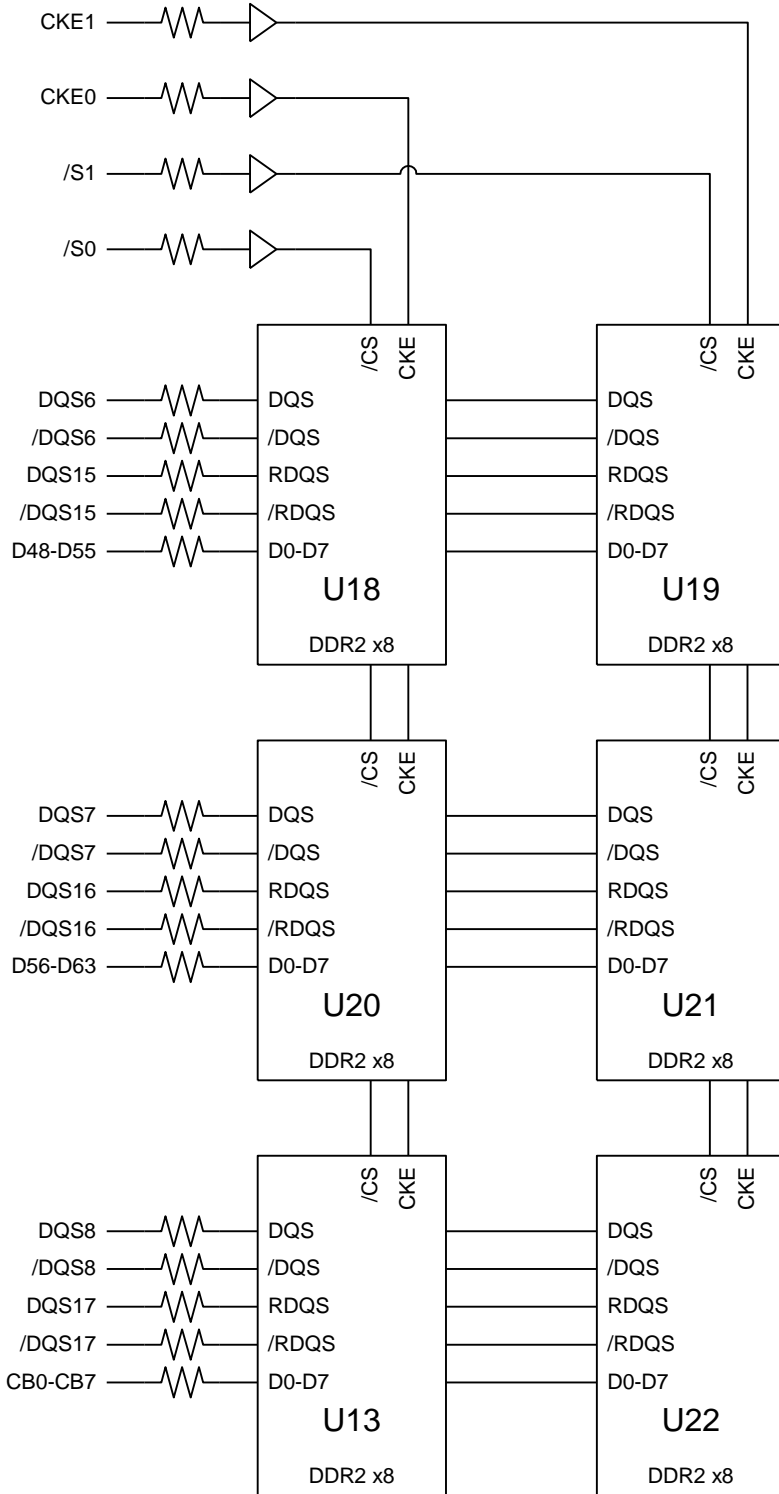
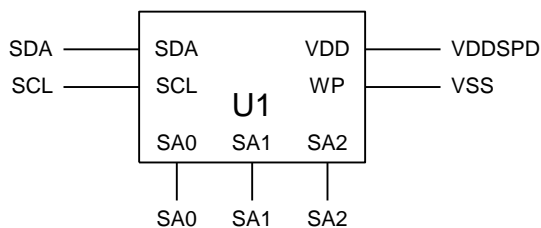
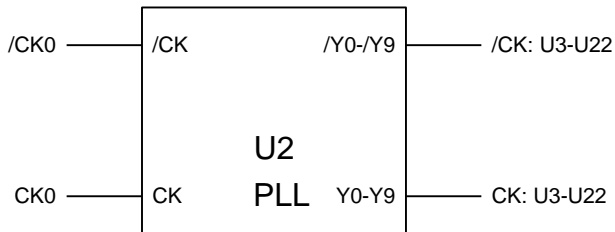
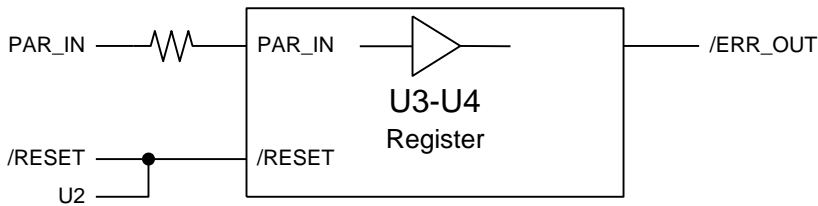
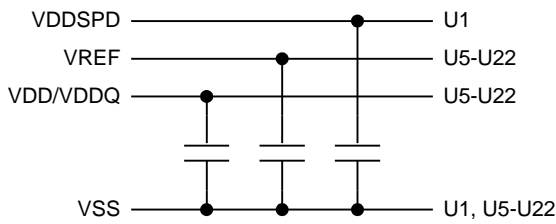
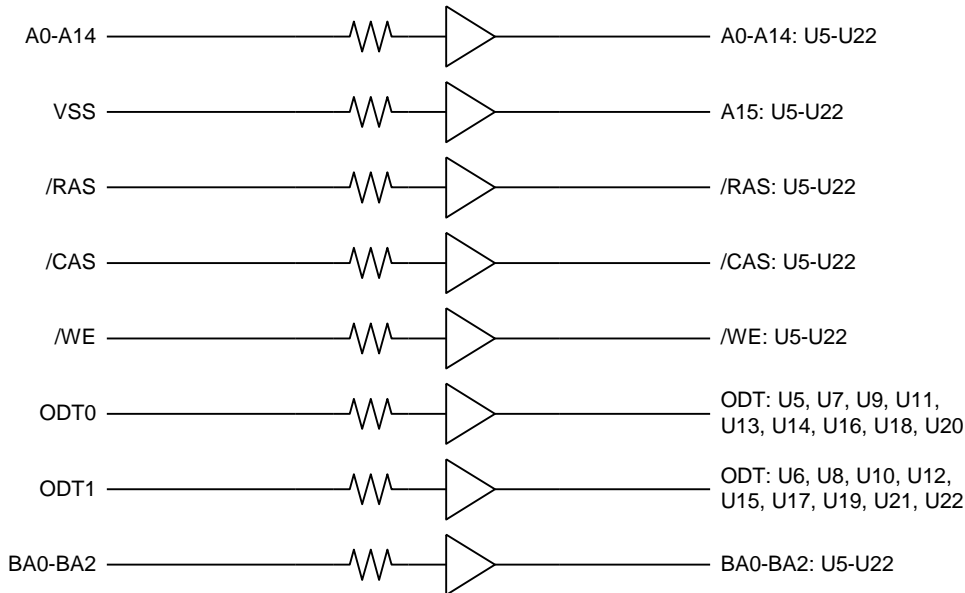


Figure 5 - Functional Block Diagram (Page 4 of 4)



Electrical Parameter

Table 8 - Absolute Maximum DC Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage on V _{DD} , pin relative to V _{SS}	V _{DD}	-1.0V ~ 2.3	V	1
Voltage on V _{DDQ} , pin relative to V _{SS}	V _{DDQ}	-0.5V ~ 2.3	V	1
Voltage on V _{DDL} , pin relative to V _{SS}	V _{DDL}	-0.5V ~ 2.3	V	1
Voltage on any pins relative to V _{SS}	V _{IN} , V _{OUT}	-0.5V ~ 2.3	V	1
Storage temperature	T _{STG}	-55 ~ 100	°C	1,2
DRAM Operation temperature (Ambient)	T _{OPER}	0 ~ 95	°C	3,4

Notes:

- 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- 3 Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51.2 standard.
- 4 At 85 - 95 °C operation temperature range, doubling refresh commands in frequency to a 32ms period (t_{REFI}=3.9 us) is required, and to enter to self refresh mode at this temperature range, an EMRS command is required to change internal refresh rate.

Table 9 - DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Rating			Units	Notes
		Min	Typ.	Max		
Supply voltage	V _{DD}	1.7	1.8	1.9	V	
Supply voltage for DLL	V _{DDL}				V	4
Supply voltage for Output	V _{DDQ}				V	4
Input reference voltage	V _{REF}	0.49* V _{DDQ}	0.50* V _{DDQ}	0.51* V _{DDQ}	mV	1,2
Termination voltage	V _{TT}	V _{REF} -0.04	V _{REF}	V _{REF} +0.04	V	3
DC input logic high voltage	V _{IH}	V _{REF} +0.125	-	V _{DDQ} +0.3	V	
DC input logic low voltage	V _{IL}	-0.3	-	V _{REF} -0.125	V	

Notes:

- 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
- 2 Peak to peak AC noise on VREF may not exceed +/-2% VREF(DC).
- 3 VTT of transmitting device must track VREF of receiving device.
- 4 AC parameters are measured with VDD, VDDQ and VDDL tied together.

Table 10 - IDD Specifications with Conditions and Operation Current

Parameter / Condition	Symbol	Current	Units	Notes
Operating precharge current; one bank active, tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD0}	756	mA	1, 2
Operating read-precharge current; one bank active, I _{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRC = tRC(IDD), tRAS = tRASmin(IDD), tRCD = tRCD(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	I _{DD1}	828	mA	1, 2
Precharge power-down current; All banks idle; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	I _{DD2P}	216	mA	1, 3
Precharge quiet standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	I _{DD2Q}	810	mA	1, 3
Precharge standby current; All banks idle; tCK = tCK(IDD); CKE is HIGH, CS\ is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD2N}	900	mA	1, 3
Active power-down current; All banks open; tCK = tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0mA	288	mA	1, 3
	Slow PDN Exit MRS(12) = 1mA	288	mA	1, 3
Active standby current; All banks open; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD3N}	990	mA	1, 3
Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD4W}	1188	mA	1, 2
Operating burst read current; All banks open, Continuous burst reads, I _{OUT} = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK(IDD), tRAS = tRASmax(IDD), tRP = tRP(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	I _{DD4R}	1323	mA	1, 2
Burst auto refresh current; tCK = tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH, CS\ is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	I _{DD5}	2880	mA	1, 3
Self refresh current; CK and CK\ at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	I _{DD6}	216	mA	1, 3
Operating bank interleave read current; All bank interleaving reads, I _{OUT} = 0mA; BL = 4, CL = CL(IDD), tRC = tRC(IDD), AL = tRCD(IDD)-1*tCK(IDD); tCK = tCK(IDD), tRRD = tRRD(IDD), tFAW = tFAW(IDD), tRCD = 1*tCK(IDD); CKE is HIGH, CS\ is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R; Refer to the following page for detailed timing conditions	I _{DD7}	1908	mA	1, 2

Notes:

- ¹ Value shown for DDR2 SDRAM only and are computed from values specified in the 2Gbit component data sheet.
- ² Value calculated as one module rank in this operating condition. All other module ranks in IDD2P (CKE LOW) mode.
- ³ Value calculated reflects all module ranks in this operating condition.

Table 11 - AC Timing Parameter and Operating Conditions

Parameter / Condition	Symbol	Min		Max		Units
		MEM512M72 D2RVD-25A1	MEM512M72 D2RVD-3A1	MEM512M72 D2RVD 25A1	MEM512M72 D2RVD-3A1	
DQ output access time from CK/CK	tAC	-400	-450	+400	+450	ps
DQS output access time from CK/CK	tDQSCK	-350	-400	+350	+400	ps
CK high-level width	tCH	0.48	0.48	0.52	0.52	tCK
CK low-level width	tCL	0.48	0.48	0.52	0.52	tCK
CK half period	tHP	Min(tCL, tCH)	Min(tCL, Tch)	-	-	ps
DQ and DM input hold time	tDH	125	175	-	-	ps
RAS to CAS delay	tRCD	12.5	15	-	-	ns
Row precharge time	tRP	12.5	15	-	-	ns
Row cycle time	tRC	57.5	60	-	-	ns
Row active time	tRAS	45	45	70000	70000	ns
Clock cycle time	tCK (CL=3)	5	5	8	8	ns
	tCK (CL=4)	3.75	3.75	8	8	
	tCK (CL=5)	2.5	3	8	8	
DQ and DM input setup time	tDS	50	100	-	-	ps
Control & Address input pulse width for each input	tIPW	0.6	0.6	-	-	tCK
DQ and DM input pulse width for each input	tDIPW	0.35	0.35	-	-	tCK
Data-out high-impedance time from CK/CK	tHZ	-	-	tAC max	tAC max	ps
DQ low-impedance time from CK/CK	tLZ	2*tAC min	2*tAC min	tAC max	tAC max	ps
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	-	-	200	240	ps
DQ hold skew factor	tQHS	-	-	300	340	ps
DQ/DQS output hold time from DQS	tQH	tHP-tQHS	tHP-tQHS	-	-	ps
First DQS latching transition to associated clock edge	tDQSS	-0.25	-0.25	0.25	0.25	tCK
DQS input high pulse width	tDQSH	0.35	0.35	-	-	tCK
DQS input low pulse width	tDQSL	0.35	0.35	-	-	tCK
DQS falling edge to CK setup time	tDSS	0.2	0.2	-	-	tCK
DQS falling edge hold time from CK	tDSH	0.2	0.2	-	-	tCK
Mode register set command cycle time	tMRD	2	2	-	-	tCK
Write postamble	tWPST	0.4	0.4	0.6	0.6	tCK
Write preamble	tWPRE	0.35	0.35	-	-	tCK
Address and control input hold time	tIH	250	275	-	-	ps
Address and control input setup time	tIS	175	200	-	-	ps
Read preamble	tRPRE	0.9	0.9	1.1	1.1	tCK
Read postamble	tRPST	0.4	0.4	0.6	0.6	tCK
Active to active command period for 1KB page size products	tRRD	7.5	7.5	-	-	ns
Four Activate Window for 1KB page size products	tFAW	35	37.5	-	-	ns
CAS to CAS command delay	tCCD	2	2	-	-	tCK
Write recovery time	tWR	15	15	-	-	ns
Auto precharge write recovery + precharge time	tDAL	WR+tRP	WR+tRP	-	-	tCK
Internal write to read command delay	tWTR	7.5	7.5	-	-	ns
Internal read to precharge command delay	tRTP	7.5	7.5	-	-	ns
Exit self refresh to a non-read command	tXSNR	tRFC+10	tRFC+10	-	-	ns
Exit self refresh to a read command	tXSRD	200	200	-	-	tCK
Exit precharge power down to any non read command	tXP	2	2	-	-	tCK
Exit active power down to read command	tXARD	2	2	-	-	tCK
Exit active power down to read command (slow exit, lower power)	tXARDS	8-AL	7-AL	-	-	tCK
CKE minimum pulse width (high and low pulse width)	tCKE	3	3	-	-	tCK

Parameter / Condition	Symbol	Min		Max		Units
		MEM512M72 D2RVD-25A1	MEM512M72 D2RVD-3A1	MEM512M72 D2RVD-25A1	MEM512M72 D2RVD-3A1	
ODT turn-on delay	tAOND	2	2	2	2	tCK
ODT turn-on	tAON	tAC(min)	tAC(min)	tAC(max)+ 0.7	tAC(max)+ 0.7	ns
ODT turn-on(Power-Down mode)	tAONPD	tAC(min)+2	tAC(min)+2	2tCK+ tAC(max)+1	2tCK+ tAC(max)+1	ns
ODT turn-off delay	tAOFD	2.5	2.5	2.5	2.5	tCK
ODT turn-off	tAOF	tAC(min)	tAC(min)	tAC(max)+ 0.6	tAC(max)+ 0.6	ns
ODT turn-off (Power-Down mode)	tAOFPD	tAC(min)+2	tAC(min)+2	2.5tCK+ tAC(max)+1	2.5tCK+ tAC(max)+1	ns
ODT to power down entry latency	tANPD	3	3	-	-	tCK
ODT power down exit latency	tAXPD	8	8	-	-	tCK
OCD drive mode output delay	tOIT	0	0	12	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	tDelay	tIS+tCK+tIH	tIS+tCK+tIH	-	-	ns

Table 12 - SPD Information

Byte NO.	Description	Note		Hex	
		MEM512M72D2RVD -25A1	MEM512M72D2RVD -3A1	- 25A1	-3A1
0	Number of serial PD Bytes written during module production	128 bytes	128 bytes	80	80
1	Total number of bytes in serial PD device	256 bytes	256 bytes	08	08
2	Fundamental memory type	DDR2 SDRAM	DDR2 SDRAM	08	08
3	Number of row addresses on this assembly	15	15	0F	0F
4	Number of column addresses on this assembly	10	10	0A	0A
5	Number of module rows on this assembly	2Rows less than 25.4mm	2Rows less than 25.4mm	01	01
6	Data width of this assembly	X72	X72	48	48
7	Reserved	-	-	00	00
8	Voltage interface level of this assembly	SSTL 1.8V	SSTL 1.8V	05	05
9	DDR2 SDRAM cycle time at maximum supported CAS Latency (CL), CL=X	2.5ns	3.0ns	25	30
10	DDR2 SDRAM access time from clock at CL=X	0.4ns	0.45ns	40	45
11	DIMM configuration type (address & command parity, data parity or ECC)	ECC with Addr and Cmd Parity	ECC with Addr and Cmd Parity	06	06
12	Refresh rate/type	7.8us, self refresh	7.8us, self refresh	82	82
13	Primary DDR2 SDRAM width	x8	x8	08	08
14	Error checking DDR2 SDRAM data width	x8	x8	08	08
15	Reserved	-	-	00	00
16	DDR2 SDRAM device attributes: Burst lengths supported	4.8	4.8	0C	0C
17	DDR2 SDRAM device attributes: number of banks on each DDR2 SDRAM device	8 banks	8 banks	08	08
18	DDR2 SDRAM device attributes: CAS Latency	5.4	5.4	30	30
19	DIMM mechanical characteristics	-	-	00	00
20	DIMM type information	Regular RDIMM (133.35mm)	Regular RDIMM (133.35mm)	01	01
21	DDR2 SDRAM module attributes	1 PLL and 1 Register	1 PLL and 1 Register	05	05
22	DDR2 SDRAM device attributes: General	Support weak driver and 50 ohm ODT	Support weak driver and 50 ohm ODT	03	03
23	Minimum clock cycle time at CL=X-1	3.75ns	3.75ns	3D	3D
24	Maximum data access time (tAC) from clock at CL=X-1	0.5ns	0.5ns	50	50
25	Minimum clock cycle time at CL=X-2	-	-	00	00
26	Maximum data access time (tAC) from clock at CL=X-2	-	-	00	00
27	Minimum row precharge time (tRP)	12.5ns	15.0ns	32	3C
28	Minimum row active to row active delay (tRRD)	7.5ns	7.5ns	1E	1E
29	Minimum RAS to CAS delay (tRCD)	12.5ns	15.0ns	32	3C
30	Minimum active to precharge time (tRAS)	45ns	45 ns	2D	2D
31	Module rank density	2GB	2GB	02	02
32	Address and command input setup time before clock (tIS)	0.17ns	0.2ns	17	20
33	Address and command input hold time after clock (tIH)	0.25ns	0.27ns	25	27
34	Data input setup time before strobe (tDS)	0.05ns	0.1ns	05	10
35	Data input hold time after strobe (tDH)	0.12ns	0.17ns	12	17
36	Write recovery time (tWR)			3C	3C
37	Internal write to read command delay (tWTR)	7.5ns	7.5ns	1E	1E
38	Internal read to precharge command delay (tRTP)			1E	1E
39	Memory analysis probe characteristics	-	-	00	00

Byte NO.	Description	Note		Hex	
		MEM512M72D2RVD -25A1	MEM512M72D2RVD -3A1	- 25A1	- 3A1
40	Extension of Byte 41 tRC and Byte 42 tRFC	tRC=57.5ns, tRFC=195ns	-	30	00
41	DDR2 SDRAM device minimum active to active/ auto-refresh Time (tRC)	57ns	60ns	39	3C
42	DDR2 SDRAM device minimum auto-refresh to active/auto-refresh command period (tRFC)	195ns	195ns	C3	C3
43	DDR2 SDRAM device maximum device cycle time (tCKmax)	8ns	8ns	80	80
44	DDR2 SDRAM device maximum skew between DQS and DQ signals (tDQSQ)	0.20ns	0.24ns	14	18
45	DDR2 SDRAM device maximum read data hold skew factor (tQHS)	0.30ns	0.34ns	1E	22
46	PLL relock time	15ns	15ns	0F	0F
47-48	DT in SPD	-	-	00	00
49	High temperature self-refresh rate support indication	-	-	00	00
50-61	IDD in SPD	-	-	00	00
62	SPD Data revision code	Rev 1.1	Rev 1.1	11	11
63	Checksum for bytes 0-62			18	6C
64-71	Manufacturer's JEDEC ID code	Manufacture's data	Manufacture's data		
72	Module manufacturing location	Manufacture's data	Manufacture's data		
73-90	Module part information	Manufacture's data	Manufacture's data		
91-92	Module revision code (For PCB& component)			0000	0000
93-94	Module manufacturing date	Manufacture's data	Manufacture's data		
95-98	Module serial number	Manufacture's data	Manufacture's data		
99-127	Manufacturer's specific data	Manufacture's data	Manufacture's data		
128-253	Open for customer use	-	-	00	00
254-255	Open for customer use	Manufacture's data	Manufacture's data	00	

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